National Science Foundation's Industry/University Cooperative Research (I/UCRC) Program

P4-25: Space Systems

Mission-Critical Computing
NSF CENTER FOR SPACE, HIGH-PERFORMANCE, AND RESILIENT COMPUTING (SHREC)

SHREC Annual Workshop (SAW24-25)

University of Pittsburgh
BYU BRIGHAM YOUNG UNIVERSITY
VIRGINIA TECH
UF UNIVERSITY of FLORIDA

January 14-15, 2025

Dr. Alan George
Mickle Chair Professor of ECE
University of Pittsburgh

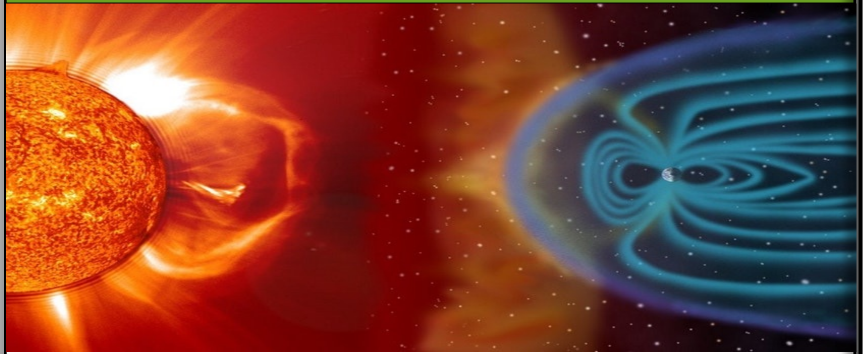
Dr. Sam Dickerson
Associate Professor of ECE
University of Pittsburgh

Mike Cannizzaro
Cole Bowman
Chris Brubaker
Dhinar Gayatri
Richard Gibbons
Mark Hofmeister
Kushal Parekh
Tom Plunkett
Graduate Students
University of Pittsburgh

Number of requested memberships ≥ 7

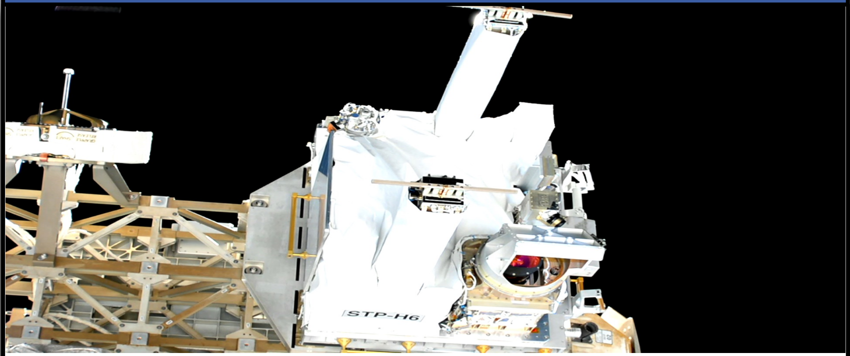
P4

Goals, Motivations, Challenges



CHALLENGES

- **Designing** and building **complex missions** with **demanding objectives** is both challenging and costly
- Novel **processors** and **architectures** require rigorous **evaluation** and **validation** to ensure appropriate **reliability** and **performance**



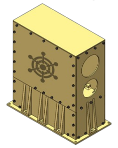
GOALS

- Research and apply **novel electrical** and **mechanical** designs and **simulations** for advanced **space missions**
- Assess **viability** and efficacy of novel **architectures** and **technology platforms** and investigate solutions based on **key criteria**: performance, SWaP, affordability, and reliability

MOTIVATIONS

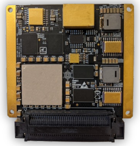
- Increased **fidelity** of modern sensors and high **computational demands** exceed capabilities of state-of-the-art **space processing**
- Need for **high-performance**, energy-efficient, **resilient**, and **affordable** onboard systems for critical missions and apps

VANTAGE



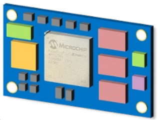
CASPR

SSP



CSP

SoMs



CPUs

GPUs

NVIDIA

Emulation

Mission-Critical Computing
NSF CENTER FOR SPACE, HIGH-PERFORMANCE, AND RESILIENT COMPUTING (SHREC)

STP-H6 Photo
This payload was integrated and flown under DoD STP - Houston leadership; photo credit NASA

SWaP: Size, Weight, and Power
CASPR: Configurable & Autonomous Sensor Processing Research
SSP: SHREC Space Processor
CSP: CHREC Space Processor
SoM: System-on-Module

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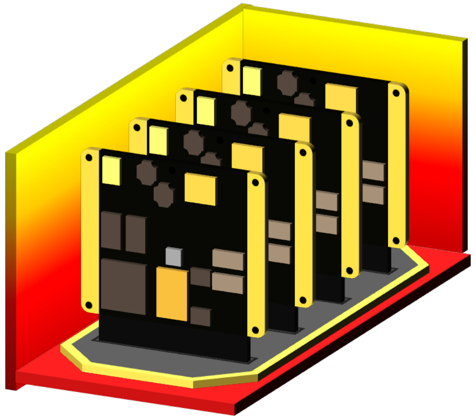
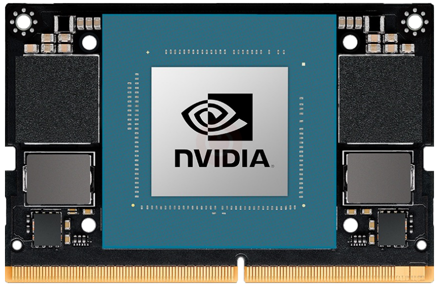
Tasks for 2025



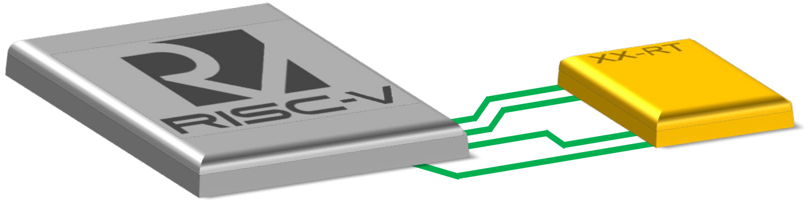
1) Onboard Flight Hardware

- Leverage hybrid systems, robust peripherals and interconnects, and efficient mechanical design to optimize space payloads



2) Space GPUs

- Investigate massively parallel architectures and apply custom dependability solutions in both hardware and software

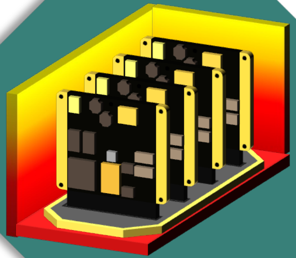


3) Space CPUs

- Evaluate fault-tolerant design approaches in silicon and systems to enhance onboard reliability and performance


4) Spacecraft and Mission Emulation

- Research system emulation and hardware-in-the-loop techniques to conduct spacecraft verification and validation



Task 1

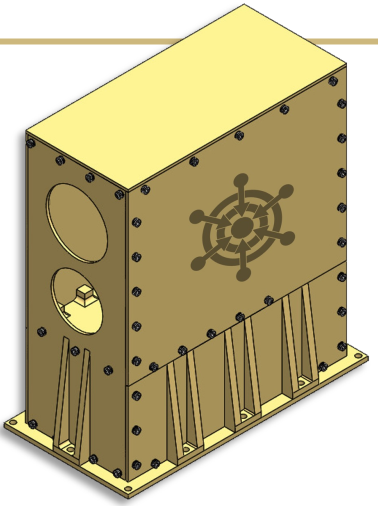
Onboard Flight Hardware

Leverage hybrid systems, robust peripherals and interconnects, and efficient mechanical design to optimize space payloads

Mark Hofmeister, Chris Brubaker, Cole Bowman, and Mike Cannizzaro

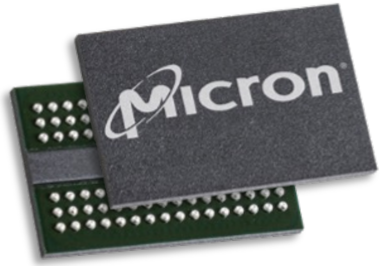
mah473@pitt.edu clb251@pitt.edu
cdb92@pitt.edu michael.cannizzaro@pitt.edu

T1: Onboard Flight Hardware



1 Space Avionics

- Kickoff **STP-H12-VANTAGE** and complete project **PDR** and **CDR** milestones
- Design and evaluate **hybrid SoM carrier** and **optical assembly** prototypes
- Measure **TID effects** on **PDNs** and **signal interconnects** and research **mitigation strategies** via novel PCB stack-ups and layouts

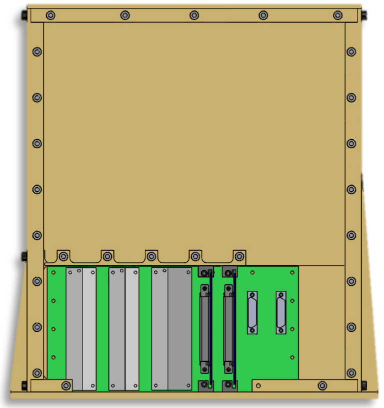


2 Robust DDR Memories

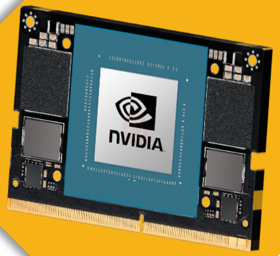
- Investigate impacts of **DDR lane width** on **throughput** and **power**
- Evaluate effect of **caching** FPGA **fabric-connected DDR4**
- Measure **performance** of hard **DDR controller** vs. soft IP

3 Mechanical and Thermal Systems

- Conduct **thermal** and **structural analyses** using simulation tools
- Evaluate **lenses** and develop camera **mounting hardware**
- Leverage **Thermal Desktop** and **ANSYS** APIs for conducting **expedited calculations**



STP:	Space Test Program
VANTAGE:	Visual and Neuromorphic Tracking and Geosensing Experiment
SoC:	System-on-Chip
PDR:	Preliminary Design Review
CDR:	Critical Design Review
SoM:	System-on-Module
TID:	Total Ionizing Dose
PDN:	Power Delivery Network
CDR:	Critical Design Review



Task 2

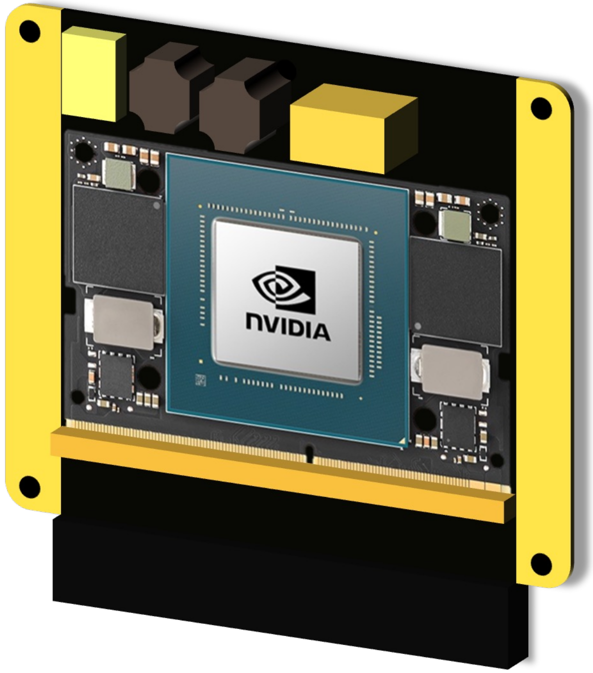
Space GPUs

Investigate massively parallel architectures and apply custom dependability solutions in both hardware and software

Tom Plunkett

thomas.plunkett@pitt.edu

T2: Space GPUs



1

Hybrid GPU SoM Carriers

- Complete **hardware designs** of radiation-tolerant and COTS **GPU SoM carriers**
- Research and develop **fault-mitigation** strategies for **NVIDIA Jetson Orin NX**

2

Tensor Core Reliability

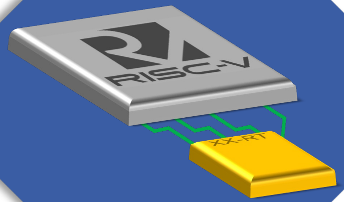
- Evaluate **image classification** and **segmentation** apps
- Characterize **Tensor Core** faults and investigate **fault propagation**
- Conduct **fault injection** on Tensor Core-enabled **ML applications**

3

Resilient Tensor Flow Integration

- Expand **RTF** to include **Tensor Core operation** functionality
- Accelerate **matrix-matrix multiply** and **2D convolution** operations
- Evaluate performance improvements of Tensor Core-accelerated apps

COTS: Commercial-off-the-Shelf
SoM: System-on-Module
ML: Machine learning
RTF: Resilient TensorFlow



Task 3

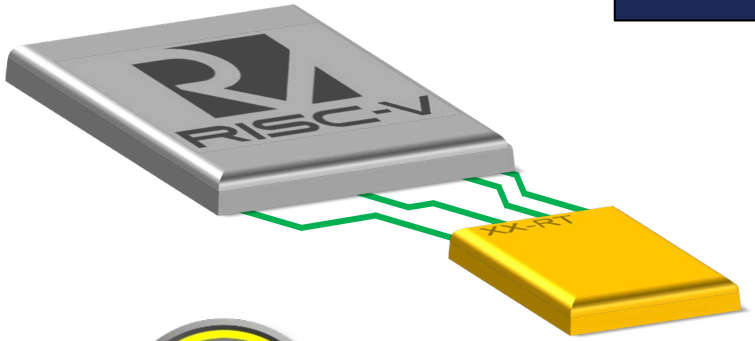
Space CPUs

Evaluate fault-tolerant design approaches in silicon and systems to enhance onboard reliability and performance

Mike Cannizzaro, Dhinar Gayatri, and Richard Gibbons

michael.cannizzaro@pitt.edu dhg13@pitt.edu
rfg17@pitt.edu

T3: Space CPUs

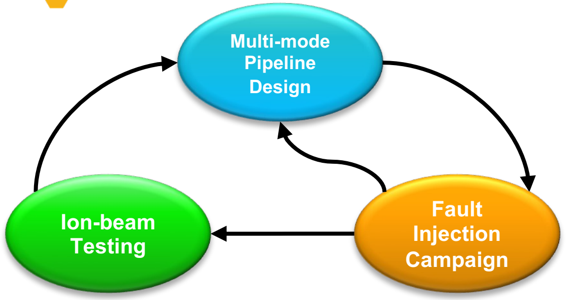


1 Onboard Coprocessors for COTS Systems

- ➢ Investigate **consolidation** of **fault-tolerant circuitry** (current monitoring, watchdog timing, etc.) into single radiation-tolerant chip
- ➢ Conduct **tradeoff study** of low-power, low-complexity **microcontrollers** and **FPGAs** for use as **coprocessor**
- ➢ Evaluate **dependability** of **standalone** processor vs. **coprocessor** pair

2 High-Performance IP Extensions

- ➢ Leverage **RISC-V vector acceleration** to optimize performance of RISC-V **softcore processors**
- ➢ **Evaluate** RISC-V vectors and **effects** on performance and power consumption in **hardcore** and **softcore processors**



3 Resilient RISC-V Chip Design

- ➢ Research impact of **dependability techniques** (TMR, lock-step, etc.) **dynamically implemented** in processor pipelines
- ➢ Synthesize **processor pipelines** for test campaigns using **Synopsys Synplify**
- ➢ **Inject faults** into pipeline designs using **Synopsys VC Z01X** and **evaluate** dependability implementations

SYNOPSYS

TMR: Triple Modular Redundancy

Task 4

Spacecraft and Mission Emulation

Research system emulation and hardware-in-the-loop techniques to conduct spacecraft verification and validation

Kushal Parekh

kup9@pitt.edu

T4: Spacecraft and Mission Emulation

1 Emulation of Spacecraft Systems

- Can **model** and **operate** compute hardware entirely in **software**
- Allows for **quick, easy testing** of spacecraft systems
- Becoming common, especially with rise of "**digital twins**"

2 Current Simulation Tools

- **Simics**
  - Cycle-accurate emulator from Intel and Wind River
- **QEMU**
  - Open-source functionally-accurate simulator

3 Renode Emulation

- Open-source emulator with industry support
- We are looking to **evaluate Renode** and **compare** it to these existing tools
- Will use **VANTAGE** as DUT for Renode evaluation

QEMU:	Quick Emulator
VANTAGE:	Visual and Neuromorphic Tracking and Geosensing Experiment
DUT:	Device Under Test

Milestones and Deliverables

➢Milestones

- SMW (June 2025): Showcase midterm results on all projects
- SAW (Jan. 2026): Demonstrate completion of all projects

➢Deliverables

- Monthly progress reports from all projects
- Midyear and end-of-year full reports from all projects
- 3-4 conference/journal papers (~1 per project)
- Hybrid carrier prototypes for Jetson Orin NX and PolarFire SoC

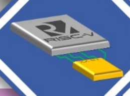
➢Budget (7+ memberships, or 350+ votes)

P4

Conclusions & Member Benefits

Leverage Novel **Systems**, **Peripherals** and **Interconnects**, and **Mechanical Designs** for Optimized **Onboard Payloads**

Investigate **Massively Parallel** Architectures and Implement Custom **Dependability** Solutions in **Hardware and Software**



Evaluate **Fault-tolerant** Designs in **Silicon** and **Systems** to Improve Onboard **Reliability** and **Performance**

Research **Emulation** and **Hardware-in-the-Loop** Techniques for Spacecraft **Verification and Validation**

➢Member Benefits

- Direct influence over research direction and projects
- Direct benefit from hardware designs, software applications, and architecture investigations
- Direct benefit from research study insights