P1-24: Reconfigurable Systems

Mission-Critical Computing
NSF CENTER FOR SPACE, HIGH-PERFORMANCE, AND RESILIENT COMPUTING (SHREC)

SHREC Annual Workshop (SAW23-24)

University of Pittsburgh · BYU Brigham Young University · Virginia Tech · UF University of Florida

January 17-18, 2024

Dr. Alan George
Mickle Chair Professor of ECE
University of Pittsburgh

Dr. Samuel Dickerson
Associate Professor of ECE
University of Pittsburgh

Dr. Peipei Zhou
Assistant Professor of ECE
University of Pittsburgh

Number of requested memberships ≥ 8

Daniel Stumpp
Ian Peitzsch
James Bickerstaff
Owen Lucas
Linus Silbernagel
Peri Hassanzadeh
Mark Ciora
Joseph Black
Research Students
University of Pittsburgh

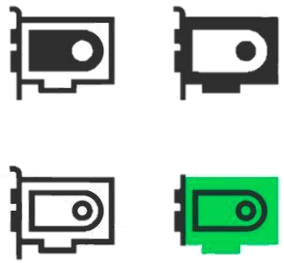
Goals, Motivations, Challenges

Goals

- Develop and evaluate **scalable architectures** for FPGA-based apps
- Compare performance of **spatial and fixed-logic architectures**
- Evaluate FPGA **design tools** for high-level synthesis

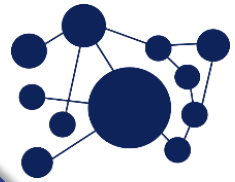
Motivations

- FPGAs realize custom datapaths for **efficient processing**
- New processing paradigms required for **increased performance**
- Potential **productivity boost** from high-level design tools



Challenges

- High-level design tools often limit **optimization granularity**
- **SWaP-C constraints** can limit parallelism due to lack of resources
- Potential **resource overhead** produced from high-level design tools

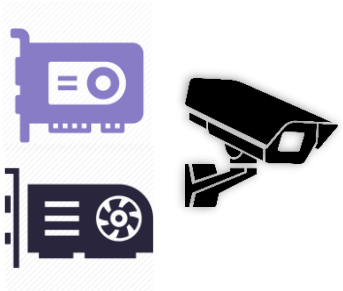


SWaP-C: Size Weight Power Cost

Proposed 2024 Tasks

T1: Neuromorphic Algorithm Accelerators

- Evaluate algorithms for **small-target tracking** in event-based remote sensing data
- Accelerate and evaluate event-based tracking on **neuromorphic processor**

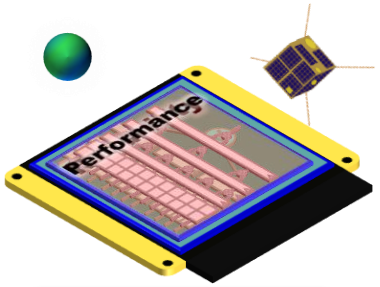


T2: High-Throughput Data Processing

- Optimize **streaming techniques** for graph & FFT processing designs
- Accelerate modern ***k*-mer counting** tools based on existing FPGA architecture

T3: Mission-Critical Sensor Processing

- Accelerate **multiple object tracking** algorithm for real-time critical apps
- Develop **RL control models** for hypersonic missile interception



T4: Machine-Learning Acceleration

- Investigate high-level FPGA **AI-acceleration** suites for hyperdimensional computing
- Evaluate **implicit neural representation** models for acceleration on Versal ACAP

T1: Neuromorphic Algorithm Accelerators

Daniel Stumpp and Linus Silbernagel

daniel.stumpp@pitt.edu
linussilbernagel@pitt.edu

University of Pittsburgh
BYU BRIGHAM YOUNG UNIVERSITY
VIRGINIA TECH
UF UNIVERSITY of FLORIDA

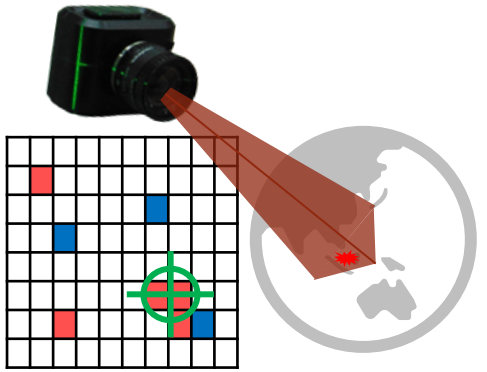
T1: Neuromorphic Algorithm Accelerators

Background

- Event-based vision sensors produce **asynchronous events** and offer unique characteristics such as high temporal resolution and high dynamic range
- Efficient processing of event streams requires custom **algorithms and accelerators**

Event-Based Small Object tracking

- Develop event-camera simulator for generation of **remote-sensing** event streams
- Leverage simulator for evaluation of algorithms for task of **real-time** point-source target **detection and tracking** in neuromorphic remote sensing data



Neuromorphic Tracking Acceleration

- Accelerate **event-based tracking** on neuromorphic processor
- Investigate power, memory, and resource utilization using SNN architectures
- Analyze performance on **Intel Loihi** and compare to traditional processors

SNN: Spiking Neural Network

T2: High-Throughput Data Processing

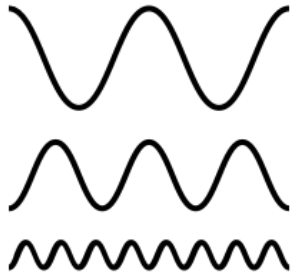
James Bickerstaff and Owen Lucas

james.bickerstaff@pitt.edu
opl1@pitt.edu

T2: High-Throughput Data Processing

Background

- Rapidly drawing insights from many large-scale datasets requires acceleration
- Emerging HLS tools allow users to leverage **increased productivity** while maintaining **high-performance** FPGA designs



Graph & Signal Processing

- Optimize multi-kernel **BFS & MST** operations through state-of-the-art streaming techniques using **oneAPI for Intel FPGAs** and next-generation devices
- Investigate methods to improve feedforward FFT **throughput and resolution**

Bioinformatics

- Investigate methods for accelerating genome sequencing for **precision medicine**
- Leverage **heterogenous computing** via high-level languages to efficiently solve high-throughput genomics tasks for next-generation sequencing

HLS: High-Level Synthesis
BFS: Breadth First Search

MST: Minimum Spanning Tree
FFT: Fast Fourier Transform

T3: Mission-Critical Sensor Processing

Peri Hassanzadeh and Mark Ciora

plh25@pitt.edu
mfc32@pitt.edu

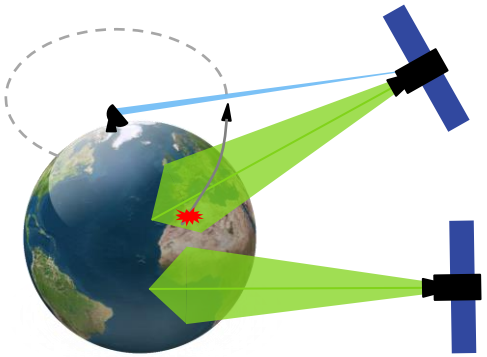
T3: Mission-Critical Sensor Processing

Background

- Advanced tracking algorithms require acceleration to sustain **many simultaneous tracks**
- Modern hypersonic missile technologies necessitate new approaches to **interceptor control** to counter **highly maneuverable** threats

Multi-Object Tracker Acceleration

- Leverage custom acceleration architecture for real-time **multiple-object tracking**
- Evaluate performance and efficiency tradeoffs for real-time **detection association and track creation** with realistic target datasets



Maneuverable Target Interception

- Design **reinforcement learning (RL)** controller models for interception of maneuverable hypersonic missiles on **SWaP-C constrained** platforms
- **Evaluate performance** of RL models and compare to traditional approaches with simulation

SWaP-C: Size Weight Power Cost
RL: Reinforcement Learning

P1

T4: Machine-Learning Acceleration

Ian Peitzsch and Joseph Black

ian.peitzsch@pitt.edu
jsb123@pitt.edu

University of Pittsburgh
BYU BRIGHAM YOUNG UNIVERSITY
VIRGINIA TECH
UF UNIVERSITY of FLORIDA

T4: Machine-Learning Acceleration

Background

- HDC offers good speedup, but accelerators seldom make use of high-level tools
- Implicit neural representations can model **discrete signals** as **continuous functions** within multilayer perceptron

Hyperdimensional Computing

- Leverage **AMD Xilinx's Vitis-AI** and **Intel's FPGA AI Suite** for HDC acceleration and compare accelerator performance
- Explore various datasets, encoding methods, and quantization levels

Implicit Neural Representations

- Explore methods for **encoding discrete signals** into implicit neural representations
- Investigate methods for encoding and reconstructing **3D objects** from image input
- Accelerate implicit neural representations methods on Xilinx **Versal ACAP**

HDC: Hyperdimensional Computing
ACAP: Adaptive Compute Acceleration Platform

Milestones, Deliverables, Budget

- **Milestones**
  - SMW (Jun/Jul 2024): Showcase midterm results on all projects
  - SAW (Jan 2025): Demonstrate completion of all projects

- **Deliverables**
  - Monthly progress reports from all projects
  - Midyear and end-of-year full reports from all projects
  - 6-8 conference/journal papers (~2 per project)

- **Budget**
  - **8+** memberships (**400+** votes) for all tasks

Conclusions & Member Benefits

- **Conclusions**
  - Develop and accelerate novel algorithms for leveraging **neuromorphic event-stream data** for tracking applications in remote sensing
  - Investigate **high-throughput applications** on novel hardware systems using oneAPI for accelerated productivity and optimized performance
  - Enable **real-time processing** of mission-critical sensor data for target tracking and interception of maneuverable targets
  - Leverage high-level tools to accelerate **novel machine learning algorithms** for various applications

- **Member Benefits**
  - **Direct influence** over research direction and projects
  - **Direct benefit** from accelerator designs and tools exploration
  - **Direct insights** from research developments and analysis