Single-Event Characterization of 16 nm FinFET Xilinx UltraScale+ Devices with Heavy Ion and Neutron Irradiation

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***Abstract*-- This study examines the single-event response of Xilinx 16nm FinFET UltraScale+ FPGA and MPSoC device families. Heavy-ion single-event latch-up, single-event upsets in configuration SRAM, BlockRAM™ memories, and flip-flops, and neutron-induced single-event latch-up results are provided.**

I. Overview

THIS study examines the single-event effects susceptibility of the Xilinx UltraScale+ Field-Programmable Gate Array (FPGA) and Multi-Processor System-on-Chip (MPSoC) device families. UltraScale+ devices are built on TSMC's 16 nm FinFET process technology. The purpose of this work is to determine the flight-worthiness and feasibility of utilizing these parts in space environments.

A Kintex UltraScale+ FPGA device and Zynq UltraScale+ MPSoC were the devices under test (DUTs). The Kintex UltraScale+ was irradiated at the Texas A&M (TAMU) K500 Cyclotron with heavy ions in May 2017. This paper presents measured single-event upset (SEU) results for the FPGA configuration memory, block random-access memory (BlockRAM™), and flip-flops, and single-event latch-up (SEL) results. The Zynq UltraScale+ MPSoC device was irradiated in neutrons at the Los Alamos National Laboratory's LANSCE facility in August and November of 2017, and SEL results are presented.

II. Test Description and Setup

A. Kintex UltraScale+ DUT

The Kintex UltraScale+ family is offered in various configurations with different numbers of logic blocks, BlockRAM, supplemental functional features (such as high-speed transceivers, digital signal processing blocks, clock management tiles, and others), speed grade, temperature grade, packaging, and I/O pin count [1]. The configuration memory in these parts is comprised of static random-access memory (SRAM) cells that control the behavior of the various internal components and the programmable interconnect.

The specific FPGA part tested was the XCKU9P-1FFVE900E-ES2, which is the final engineering silicon release of the Kintex UltraScale+ contained within a flip-chip package. This particular device is comprised of the following features [1]:

- 548,160 Flip-flops
- 274,080 Look-up tables for combinatorial logic
- 912 BlockRAM modules (36 Kb each)
- 4 Clock management tiles
- 2,520 Digital signal processing slices
- 1 System monitor (ADC)
- 28 GTH Transceivers (up to 16.3 Gb/sec)

Brigham Young University's JTAG Configuration Monitor (JCM) [2], a Xilinx Zynq-based module that connects to the DUT FPGA JTAG chain, was used to interface to the DUT configuration memory. Using this device, a user can log into an embedded Linux environment and execute sequences of JTAG commands to program, read back, and scrub the configuration memory of the DUT. The JCM was to detect and correct SEU events as they occurred during irradiation.

The backside silicon of the Kintex UltraScale+ FPGA DUTs was thinned to approximately 60 μm and the parts were soldered to a basic test board that had individual power inputs for each independent voltage rail on the device as well as JTAG, SelectMAP, and a small number of high-performance and high-density general-purpose I/O pins. A picture of the test board is below in Fig. 1.

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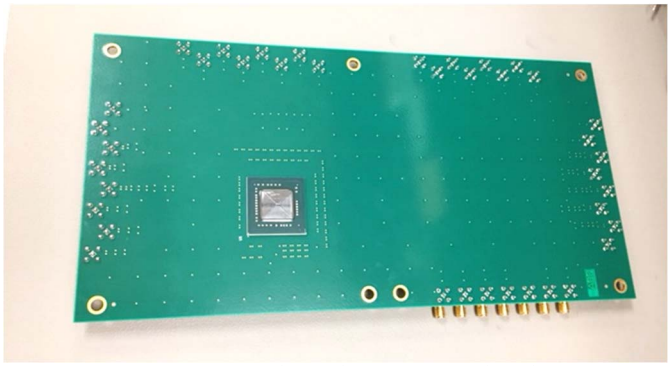

Fig. 1. Kintex UltraScale+ DUT on test board.

Kintex UltraScale+ devices operate with a nominal 0.85 V main core voltage (VCCINT and VCCINT_IO), an auxiliary voltage of 1.8 V (VCCAUX and VCCAUX_IO), high-density I/O pins using supply voltages from 1.2 V up to 3.3 V (VCCO_HD), high-performance I/O pins at voltages of 1.0 V to 1.8 V, and other voltage rails to support secondary features in the device (VCCBRAM, VBATT, VCCADC, and MGT voltages for SERDES). The KU9P DUT board was powered through a Keysight N6705B power analyzer with four independent channels configured and connected as follows:

- Channel 1: 0.85V, VCCINT
- Channel 2: 1.8V, VCCAUX, VCCAUX_IO, and VCCADC
- Channel 3: 0.85V, VCCBRAM and VCCINT_IO
- Channel 4: 1.8V, VCCO_HD and VCCO_HP

The encryption circuitry (powered by VBATT), as well as the high-speed SERDES/MGTs (powered by MGTAVCC, MGTAVTT, and MGTVCCAUX) were grounded for this experiment.

B. Zynq UltraScale+ MPSoC DUT

The Zynq UltraScale+ MPSoC device incorporates the same style of programmable fabric as the Kintex UltraScale+ in a portion of the device labeled the "Programmable Logic" (PL). Addionally, the MPSoC incorporates a "Processor Subsystem" (PS) that is comprised of multiple ARM processors, GPU, and a host of supporting peripheral IP.

The specific MPSoC part tested was the XCZU9EG-2FFVB1156I. This part is comprised of the following features [3]:

Processing Subsystem:

- Quad-core ARM Cortex-A53 Application Processing Unit
- Dual-core ARM Cortex-R5 Real-Time Processing Unit
- 256 KB on-chip memory with ECC
- ARM Mali-400 GPU
- Integrated memory and DMA controllers
- 4 High-speed serial transceivers (6.0 Gb/sec)
- Supporting IP (PCI Express blocks, SATA, DisplayPort controller, Ethernet MACs, USB, CAN, SPI, SDIO, UART, etc.)
- Management units for power gating, configuration, and security
- PS System monitor ADC

Programmable Logic:

- 548,160 Flip-flops
- 274,080 Look-up tables for combinatorial logic
- 912 BlockRAM modules (36 Kb each)
- 4 Clock management tiles
- 2,520 Digital signal processing slices
- PL System monitor ADC
- 24 GTH Transceivers (up to 16.3 Gb/sec)

The ZU9EG part was mounted to a commercially available development board from Xilinx, the ZCU102. A picture of the ZCU102 is below in Fig. 2.

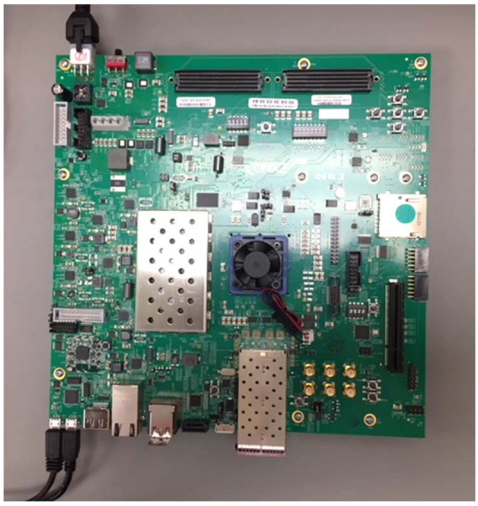

Fig. 2. ZU9EG DUT (under heatsink) on ZCU102 evaluation test board.

The ZU9EG power scheme is more complex than the KU9P device; it has all of the same power rails as the KU9P to power the PL side of the device, but also contains a number of power inputs for the PS. The majority of these power rails are powered at 0.85 V (full- and low-power domain core voltages, DDR controller, and SERDES supply). The PS auxiliary supply, system monitor, and SERDES termination voltages are powered at 1.8 V. The I/O voltages range from 1.2 to 3.3 V.

In an initial attempt to power the device using the on-board regulators of the ZCU102 for neutron testing, it was discovered that several of the power regulators on the board were susceptible to neutrons, resulting in visible damage to the regulators and the ZU9EG device. To alleviate this issue so that the device power could be monitored to evaluate potential current events, the power regulators had to be bypassed. This was done by disconnecting the power regulator outputs and soldering wires to banana jacks that allowed the current and voltage of each output channel to be supplied and monitored from an external power supply, as shown below in Fig. 3 and

Fig. 4. The four channels were connected to the following power rails of the ZCU102 board as follows:

- Channel 1: 3.3V, VCC3v3 and UTIL_3V3
- Channel 2: 0.85V, VCCBRAM, VCCINT, VCCPSINTFP, and VCCPSINTLP
- Channel 3: 1.2V, DDR4_DIMM_VDDQ
- Channel 4: 1.8V, VCCAUX and VCCOPS

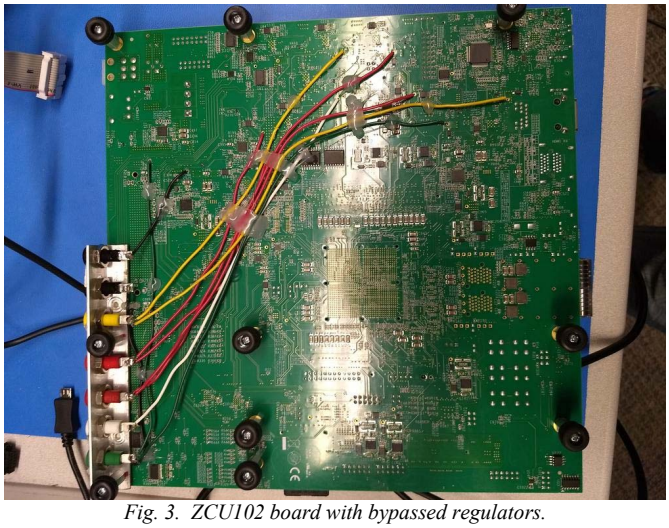

Fig. 3. ZCU102 board with bypassed regulators.

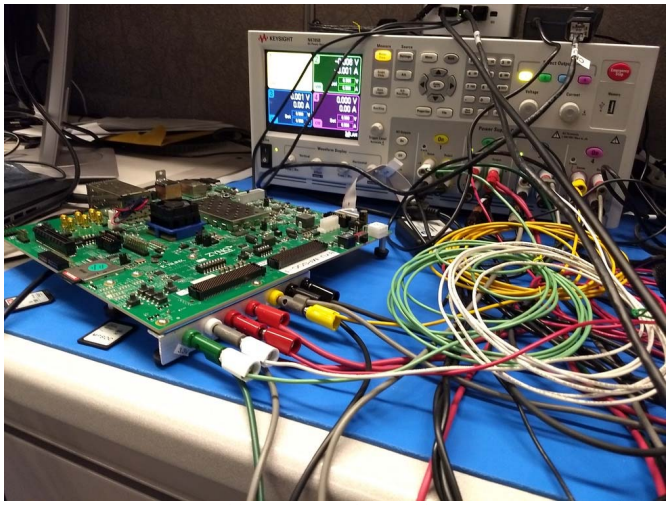

Fig. 4. ZCU102 powered by an external Keysight N6705B Power Analyzer.

C. Heavy Ion SEU Test Parameters

The Kintex UltraScale+ DUTs were irradiated in air at TAMU using 15 MeV/μ neon and argon. With an air gap of 7.4 cm, a 25.4 μm aramica window, and aluminum degraders, irradiation with neon yielded LETs from 3.2 to 6.0 MeV-cm^2/mg, and argon yielded LETs of 10.6 to 20.1 MeV-cm^2/mg. All irradiation was performed at normal incidence, nominal voltage biases, and at room temperature. A picture showing the test setup follows in Fig. 5.

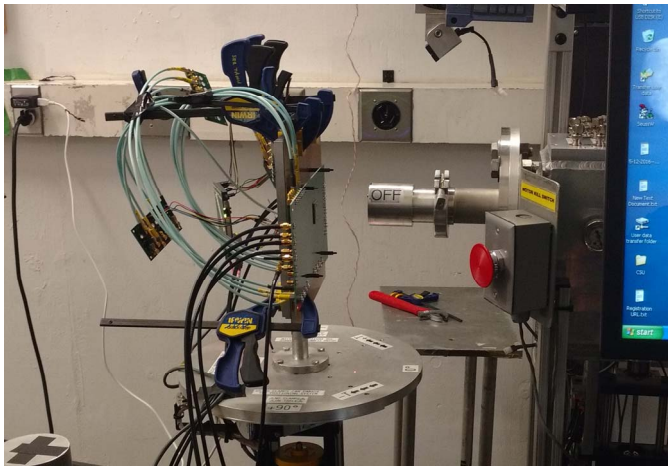

Fig. 5. Test setup of KU9P DUT board at TAMU K500 Cyclotron.

The goal of SEU testing was to examine the static SEU response of the configuration SRAM, BlockRAM memories, and the user flip-flops in the Kintex UltraScale+. During irradiation, the clock was stopped, which masked most dynamic effects typically caused by single event transients. The post-irradiation state of the DUT was compared to the starting state to yield static upset counts.

To obtain flip-flop and BlockRAM upset rates, specific memory values were pre-loaded into the device through the configuration bitfile. 50% of the available flip-flops were built into multiple flip-flop chains, preloaded with either an "all-0s" or "all-1s" pattern. The resets connected to these flip-flops were configured to either reset or preset such that any reset transients would always flip the value of the cell opposite of its initialized value. The FPGA design also included 100% of the BlockRAMs resources in the DUT, half preloaded to "1" values and the other half with "0" values.

Following FPGA configuration, the clock was stopped and the part was irradiated until conditions arose that required stopping the beam, typically due to temperature or current exceeding safe levels. During irradiation, the device was constantly being read back and results stored to disk, providing multiple readbacks which each represented the device state over a short time span. These readbacks were individually analyzed and the results accumulated to obtain enough events for statistical significance and to reduce the incidence of two coincident SEUs on the same memory cell from masking events.

Once the beam was turned off, a final readback command was issued to record the final state of the configuration and BlockRAM memories. Following this, a "capture" command was issued to the FPGA which stores the state of all user flip-flops into the configuration memory. The configuration memory is then read back one last time to get the current state of the flip-flops. The post-capture readback is only used for flip-flop data, as this command also causes changes to other unrelated portions of the configuration memory, and thus should not be included in any final upset counts, as these memory changes were not SEU-induced.

D. Heavy Ion SEL Test Parameters

SEL testing was performed concurrently with SEU testing, thus the conditions relating to the SEL results are the same as described in the previous section.

Whenever a SEL event was detected, the beam was stopped until the latch-up site could be cleared out. The run was only stopped when a significant number of events (SEU or SEL) were obtained or when the device was no longer functional for any reason (typically due to current limiting causing voltage droop and internal DUT brown-out circuitry to activate).

E. Neutron SEL Test Procedure

The Zynq UltraScale+ MPSoC DUTs were irradiated in air at the Los Alamos National Laboratories LANSCE facility to a fluence of 3.09×10^{11} ions. A picture of the test setup follows in Fig. 6.

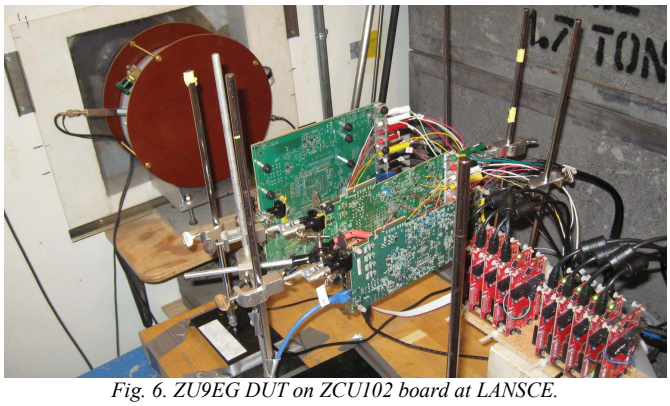

Fig. 6. ZU9EG DUT on ZCU102 board at LANSCE.

There were two designs of this test. In both instances, following power-up of the DUT, the device was configured and placed into operation before irradiation.

The initial design of this test utilized the external power supply to mitigate latch-up on the MPSoC when a power event was detected. The objective of this test was to monitor the power on the board and determine the extent of the current events and the issues they pose.

Later, a second test was performed to attempt self-monitoring and self-mitigation of latch-up events. During this test, an unmodified ZCU102 board was utilized such that the ARM Cortex-R5 could communicate with the on-board power regulators through a PMBUS interface. This interface could be used for power monitoring and subsequently to power cycle potentially latched-up power rails. The objective of this test was to further understand the danger of longer-term persistence of SEL events, evaluate effectiveness of on-board mitigation, and analyze wear on the chip due to these high current events.

III. Results

A. Heavy Ion Configuration Memory Cell SEU

To determine upset counts, the readback files obtained from the JCM were compared to the original bitfile that was used to program the device initially before irradiation. Additionally, the Xilinx software tools provide a mask file, which indicates which bits in the bitstream are pertinent to the operation of the design loaded in the device. To ensure that the bits being examined were pertinent to device operation, and not a part of some other resource (such as BlockRAM), only the bits indicated as essential bits by the mask file and not indicated as a flip-flop or BlockRAM resource, were evaluated. For this test design, this resulted in 118,502,560 bits examined out of a total initial bitstream size of 212,068,240 bits.

The Weibull curve illustrating the configuration memory cell cross-section is shown in Fig. 7. The number of events at the LET=15 and 20 MeV-cm^2/mg points was low (8 and 4 events, respectively), yielding some uncertainty towards the right side of the curve. Obtaining data at these higher LETs was difficult due to SEL response. Given the available data, the Weibull fit was made rather pessimistically, to fit the potential worst-case scenario.

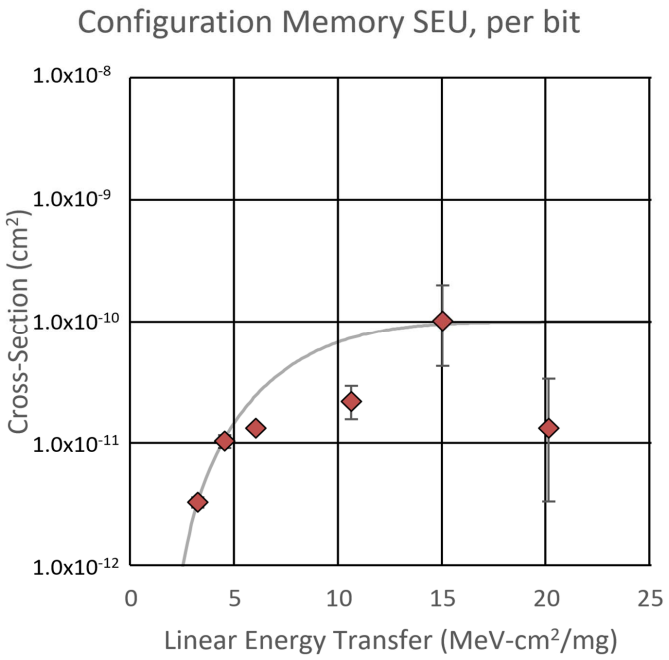

Fig. 7. Weibull curve for configuration memory cell upsets, per bit. Error bars that are smaller than the marker symbol may not be visible. The Weibull parameters are L_{th}=1.5 [MeV-cm^2/mg], σ_{sat}=0.01 [μm^2/bit], W=8.0 [MeV-cm^2/mg], S=2.2.

A final examination of the configuration cells looked at memory locations storing a '0' value compared to those storing a '1' value. The unmasked configuration bitstream was comprised of 113,945,174 '0' values and 4,557,386 '1' values. After normalizing the SEU data, the cells storing '0' values tended to upset more often than stored '1' values by a ratio of about 1.91:1.

Overall, the SEU performance of the 16 nm FinFET configuration memory cell is a significant improvement from previous Xilinx device families, even when considering improvement that typically comes with feature size scaling. A comparison of previous devices using data from [4]-[7] is shown below in Fig. 8 and in Table I. The event rates in Table I are from CREME96 [8] and assume a geosynchronous orbit, solar minimum conditions, and 100 mils of aluminum shielding.

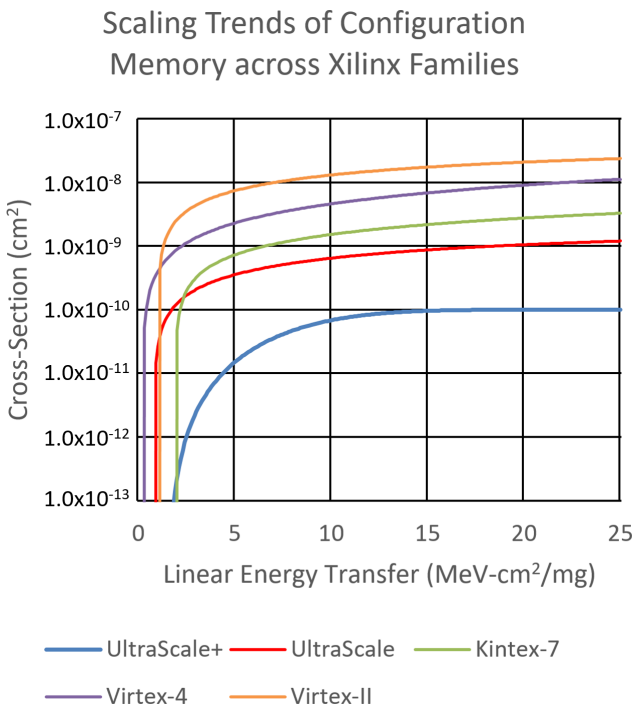

Fig. 8. Scaling trends across previous generation Xilinx device families.

TABLE I
SCALING TRENDS COMPARED BY UPSET RATE PER BIT

Family	Technology Node	Upset rate
Virtex-II	130 nm bulk	3.99E-07
Virtex-4	90 nm bulk	2.63E-07
Kintex-7	28 nm bulk	1.41E-08
UltraScale	20 nm bulk	7.56E-09
UltraScale+	16 nm FinFET	9.18E-12

(per bit, per day)

B. *Multiple Cell Upsets in Configuration Memory*

Though most upsets are Single-Cell Upsets (SCUs) affecting only one memory bit, Multiple-Cell Upsets (MCUs) may also occur when a single particle causes two or more physically-adjacent cells to upset. This is of concern to Xilinx FPGAs which are protected by a Single-Error Correct, Double Error-Detect (SECDED) Error Correcting Code (ECC), as single events that cause MCU resulting in two bits in the same word to upset would break the ECC scheme. For this analysis, a statistical method described on [9] was applied to extract information of the MCUs on the SEU data set.

The FPGA configuration memory is divided into large addressable memory words, called frames, that are 2,976 bits per frame and protected with SECDED ECC. To analyze the readbacks for MCU, the entire bitstream was analyzed and each upset observed is translated into (u,v) coordinates, where u is the frame number and v is the bit number within the frame. Then, the method iterates through each upset and looks within a vicinity for other upsets. For our case, the length of the vicinity is +32 to -32 frame addresses or bits. For any other upsets in this vicinity, the offset is computed between each upset pair and these results are binned. Offsets are designated by (x, y), where x = the offset in configuration frames (zero indicates the two upsets are in the same frame), and y = the offset in bit positions within a frame. Bins with significantly higher counts than others suggest physical adjacency between upsets. Table II shows the percentages of the shapes created by the common offsets. The last column shows the total number of upsets, i.e., the sum of MCUs and SCUs.

The overall cross-section for the MCU events is presented in Table III. The cross-section of SCUs is consistent between both ions. The cross sections of MCUs of size 2 are one order of magnitude below that of SCUs. Likewise, the cross-section of MCUs of size 3 is at least two orders of magnitude below that of SCUs. The probability of occurrence of an MCU is small and becomes smaller as the size of the MCU increases.

TABLE III
CROSS-SECTION OF SCUS AND MCUS OF SIZE TWO AND THREE

Ion	SCU	MCU 2	MCU 3
Ar	8.29E-03	6.59E-04	2.79E-05
Ne	8.03E-03	1.04E-04	8.81E-06

A heat map focused on the most common offsets is shown in Fig. 8. From the heat map, the common offsets observed from analysis are illustrated: (0,-8), (1,0), (3,-1), and (7,-2).

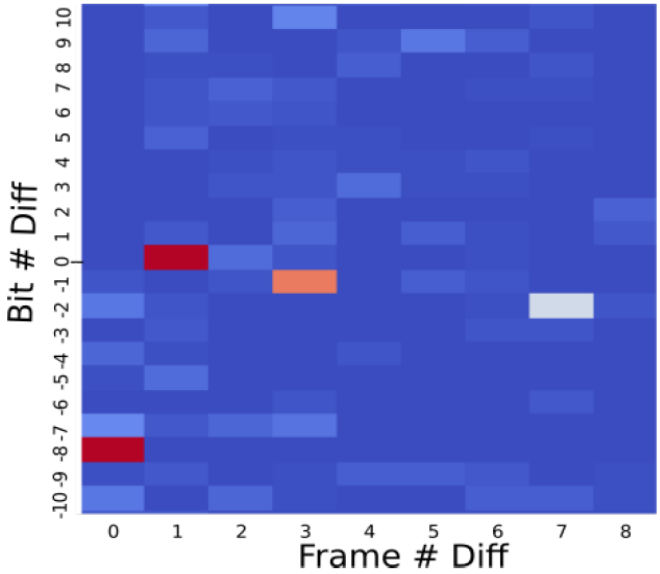

Fig. 9. Heat map representing the more common pair offsets. Blue is least occurring, red is most prevalent.

TABLE II
PERCENTAGES OF MCUS EXTRACTED FOR ARGON AND NEON IONS BY SHAPE

ion	(1,0)	(0,-8)	(7,-2)	(3,-1)	(0,-8),(0,-8)	(1,0),(1,0)	(1,0),(3,-1)	total upsets
Ar	4.89%	0.67%	0.57%	0.67%	0.19%	0.00%	0.10%	**1044**
Ne	0.41%	0.68%	0.06%	0.11%	0.11%	0.00%	0.00%	**70305**

To minimize the chance that a pair of independent SEUs would create a "fake MCU" when they are physically adjacent (called Coincident SEUs, or CSEUs), only readbacks with a low number of SEUs per readback we used in order to minimize the probability of CSEUs contaminating the data. Fortunately, the frequent readback by the JCM during irradiation makes the probability of a CSEU extremely low.

C. *Heavy Ion Flip-Flop SEU*

The flip-flop SEU response is shown below in Fig. 10. Flip-flop upsets were very difficult to obtain at the higher LETs due to SEL response; only one event was observed at an LET=15 MeV-cm^2/mg, and no events observed at LET=20 MeV-cm^2/mg as more fluence was needed. It should be noted that a change in value could be caused by either a SEU on the memory cell itself, or from a single-event transient on a reset line, which would cause the bit to flip to the opposite of its initialized value.

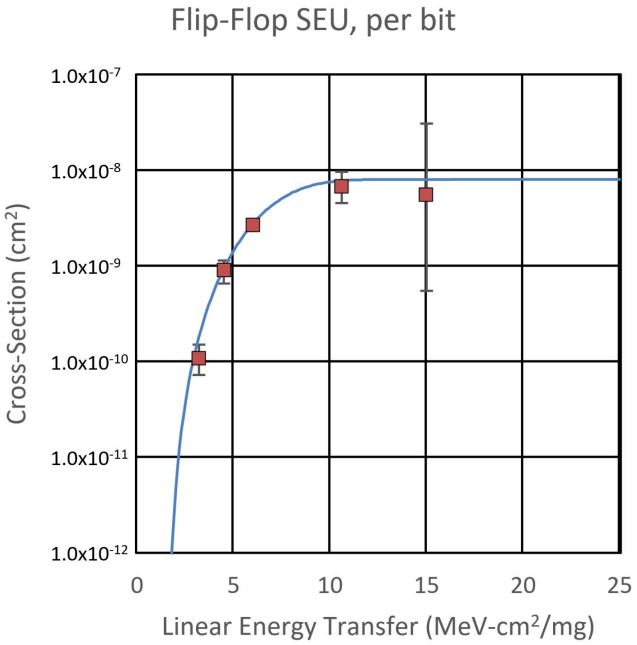

Fig. 10. Weibull curve for flip-flop upsets, per bit. Error bars that are smaller than the marker symbol may not be visible. The Weibull parameters are L_{th}=1.5 [MeV-cm^2/mg], σ_{sat}=0.8 [μm^2/bit], W=6.0 [MeV-cm^2/mg], S=3.

The flip-flop chains were comprised of 137,040 cells initialized to '0' values and 137,040 initialized to '1' values. The cells storing '0' values tended to upset more often than stored '1' values by a ratio of about 2.34:1.

D. *Heavy Ion BlockRAM SEU*

The BlockRAM SEU response is shown below in Fig. 11.

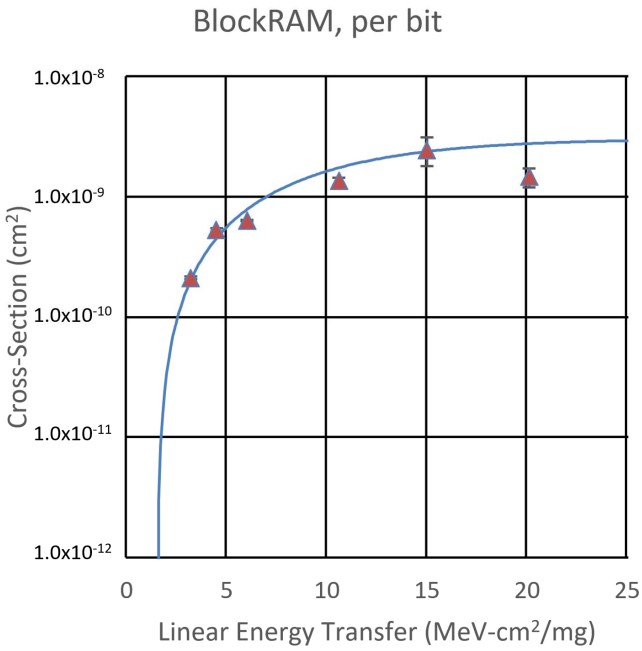

Fig. 11. Weibull curve for BlockRAM upsets, per bit. Error bars that are smaller than the marker symbol may not be visible. The Weibull parameters are L_{th}=1.5 [MeV-cm^2/mg], σ_{sat}=0.3 [μm^2/bit], W=10.0 [MeV-cm^2/mg], S=1.5.

The BlockRAM bits were comprised of 16,809,984 bits initialized to '1' and 16,809,984 initialized to '0'. There was no apparent bias in upsets between cells storing '0's or '1's.

E. *Heavy Ion SEL Results*

In the SEL beam runs, a high-current anomaly was observed on the VCCAUX supply rail across all LETs in heavy ions. This anomaly resulted in a destructive event to one DUT when the event was allowed to remain in the device and when no current limit was set on the VCCAUX rail. Following a presumed SEL on VCCAUX, other rails showed SEL-like behavior, likely due to the concentrated localized heating from the VCCAUX event inducing other latch-up sites. Fig. 12 is a current trace over time of the four supplies used to power the DUT. The nominal operating current is that at the far left of the graph, where all supplies are well below ~0.5 amps. The current limit on VCCO was set to 2 amps (resulting in the 2 A plateau that begins near t=20 sec), while all other supplies had current limits set at 10 A.

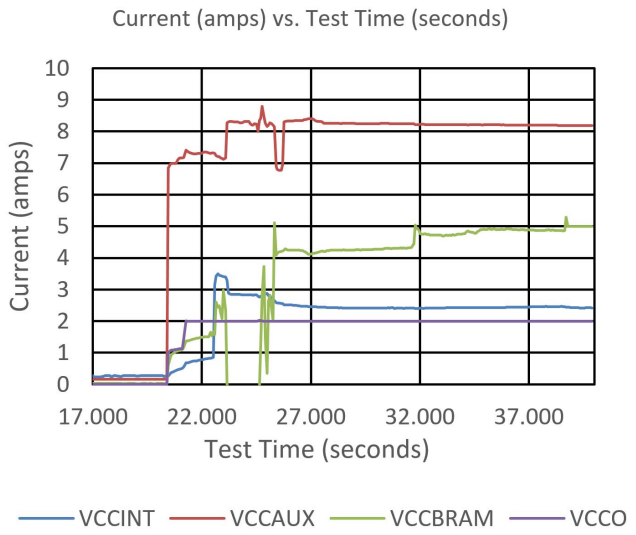

Fig. 12. Current strip chart taken during a SEL test run at TAMU showing a destructive event that began with high current on VCCAUX.

When the VCCAUX supply was limited, the events were non-destructive allowing a more statistically significant number of events to be observed. During this extended testing, no other voltage rails showed any high-current abnormalities. Despite the ability to current-limit the SEL events, more data points are desired and future test trips shall prioritize this to improve the statistical significance of these data.

It should also be noted that due to the shutter response time to stop the beam at the TAMU K500 cyclotron, there is a brief delay in event detection to the beam turning off. Because of this, the fluence numbers are slightly elevated, which would make these results somewhat undesirably optimistic. The SEL data form the Weibull curve below in Fig. 13.

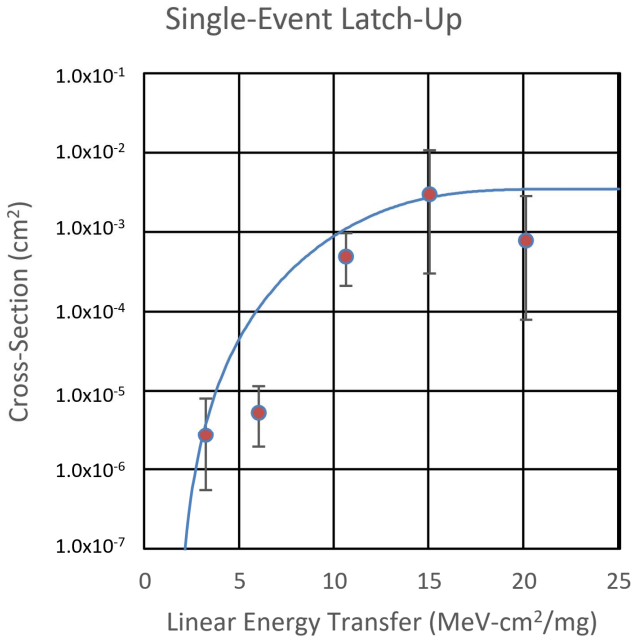

Fig. 13. Weibull curve for single-event latch-up events. The Weibull parameters are L_{th}=1.5 [MeV-cm²/mg], σ_{sat}=3.5x10⁵ [μm²/bit], W=12.0 [MeV-cm²/mg], S=3.5.

F. Neutron SEL Results

The first neutron test involved the use of external supplies to power the ZCU102 test board during irradiation. Initial testing showed various power events occurring on the board including voltage spikes, current spikes as shown in Fig. 14, and a positive jump in current. Further investigation showed that some of the current "spikes" that were observed were actually a spike followed by a high but stable current.

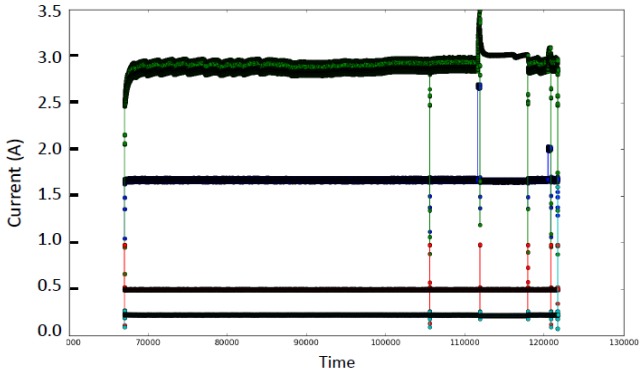

Fig. 14. Current plot of one test segment. Change in current was 600 mA on the top plot and 1 A on the upper-middle plot.

Based on the results, it appears that the susceptible power lines are the VCCAUX 1.8 V line and the VCCINT 0.85 V line as those two lines were the only power lines that reported errors. The VCCAUX line is the most susceptible line as it was the problem power rail for the majority of the reported events. On average, a current event causes an increase of 330 mA on the particularly affected line, while some events are more extreme, such as the one that was shown in Fig. 14. Generally, when VCCAUX was affected by an event, VCCINT was also affected, and vice versa. The power results for the MPSoC are shown in Table IV.

TABLE IV
POWER EVENT CROSS SECTION RESULTS

	Num Err	Fluence	Cross Section	σ Error
VCCAUX	25	3.09E+11	8.09E-11	3.24E-11
VCCINT	1	3.09E+11	3.24E-12	6.47E-12
Total	26	3.09E+11	8.42E-11	3.30E-11

A second test was performed that attempted to detect and recover from the SEL utilizing an unmodified ZCU102. The ZCU102 was connected to a large uninterruptible power supply (UPS) to guarantee that the current event would be "captured" and not lost due to a loss in power. The ARM Cortex-R5 was running software that used the built-in system monitor (SYSMON) and communicated with the power regulators through PMBus to monitor the temperature of the chip and the current of the susceptible voltage lines. This software would send a I/O signal to request a reboot of the board when an event was detected. Once a current event was "captured" on the MPSoC, attempts were made to mitigate the event without repowering the board. These attempts included resetting the processor, performing a power-on reset, and sending JTAG reset commands. None of these attempts

proved successful and an event only seems to be resolved through a complete power cycle of the board.

The results of this test show that the mitigation software was successful in detecting current events and could successfully send an external signal to request reboot; however, the current results show many false-positive requests in addition to the actual requests. Through more testing of this software, a reliable detection model is most likely achievable. This test also showed that communication to the MPSoC board can be lost in some of the high current events. Communication through UART and JTAG were lost on many (but not all) of the current events, implying that several different latch-up sites may be present in the device.

IV. Space Event Rates for Heavy Ion Data

CREME96 [9] was run on the heavy-ion data to determine sample spacecraft rates for operation in a GEO orbit under solar minimum conditions, 100 mils of aluminum shielding, and disregarding direct proton ionization effects (Z=2-92). The resulting rates are given in Table V.

TABLE V
CREME96 Event Rates

	Per bit	Per device		
	Upsets/day	Upsets/day	Days/upset	# of Elements
Configuration RAM	9.18E-12	0.00164	611.2	178,189,952
Flip-Flops	2.08E-08	0.0144	69.3	548,160
BlockRAM	5.29E-09	0.178	5.6	33,619,968
Single-event Latch-up	1.48E-02	0.0148	67.6	-

V. Conclusion

The Kintex UltraScale+ FPGA parts were tested for SEU and SEL performance in heavy ions at TAMU at effective LETs from 3.2 to 20.1 MeV-cm^2/mg. The Zynq UltraScale+ was tested for SEL at LANSCE in neutrons to a fluence of 3.09×10^{11} ions.

SEU cross sections are presented and performance of the part yielded excellent results consistent with expectations derived from combining previous Xilinx FPGA family SEU performance with transistor feature size scaling.

During SEL testing in both heavy ions and neutrons, the UltraScale+ exhibited high current anomalies typically starting on the VCCAUX rail. This current anomaly had a significant effect, raising current levels by up to several amps, and yielding both destructive and non-destructive effects.

VI. References

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