Synchronization Issues of TMR Crossing Multiple Clock Domains

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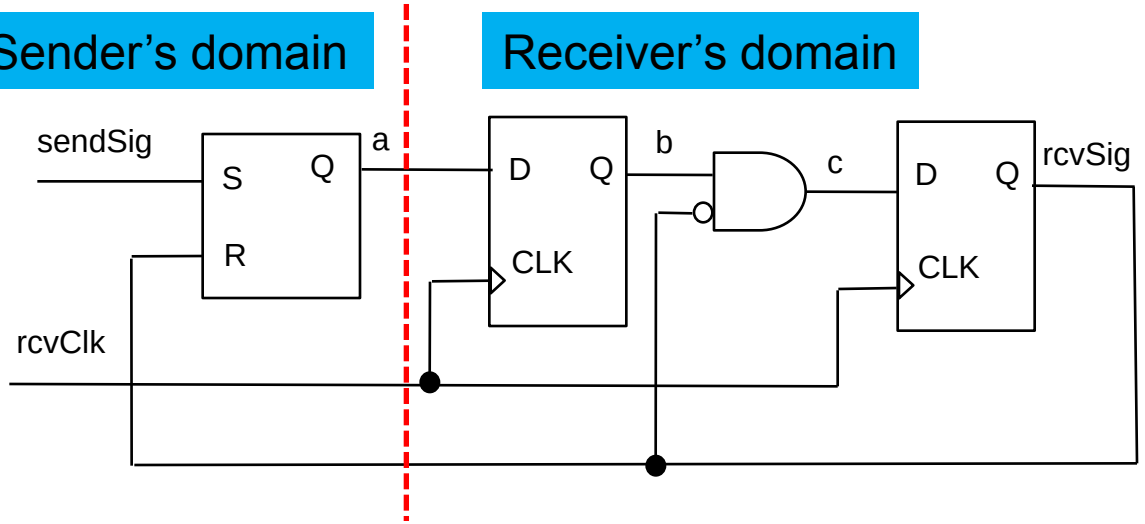
Introduction

- TMR suffers from 3 issues when crossing clock domains
  1. Meta-stability causes problems when asynchronously sampling
  2. Sampling uncertainty is inevitable when sampling asynchronous signals
  3. SEUs exacerbate the effect of sampling uncertainty resulting in lower reliability

Issue #1: Meta-stability



Resolution time $T_r = T_{clk\_receiver} - T_{pd}$

$$MTBF = \frac{e^{K_2 T_r}}{K_1 F_s F_r}$$

Example:

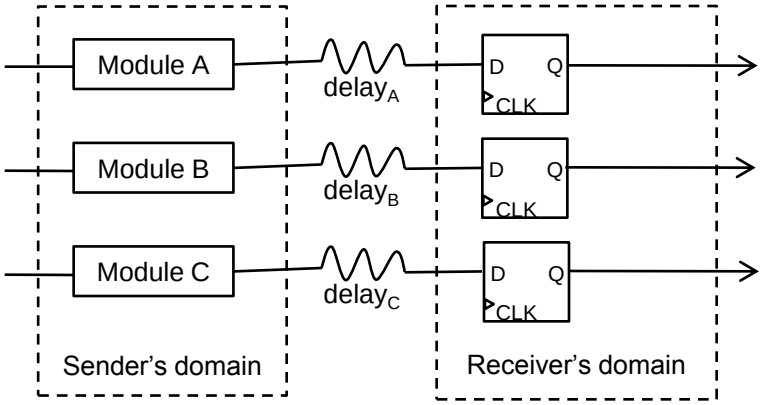
K_1=0.1ns, K_2=24.3/ns (Xilinx Virtex 4),
F_s=100MHz, F_r=333MHz, T_{pd} = 0.5ns

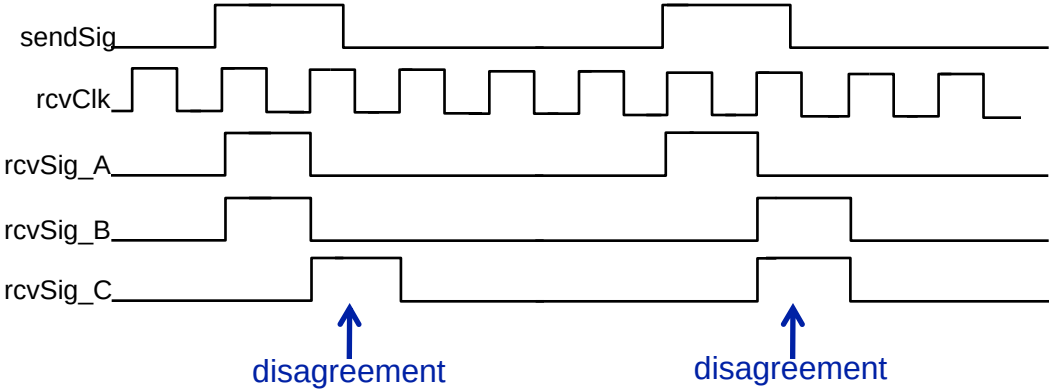
MTBF = 2.3×10^{12}years

Reference: Peter Alfke, "Metastable delay in Virtex FPGAs", tech. report, Xilinx, 2008

Issue #2: Sampling Uncertainty

- Sampling uncertainty is inevitable when sampling asynchronous signals
  - Even with balanced delays on the 3 interconnect legs, signals arrive in receiver's domain on different cycles





$$\#\ \text{disagreements/sec} = \frac{d_{max} - d_{min}}{i} \times F_s \times F_r$$

Example:

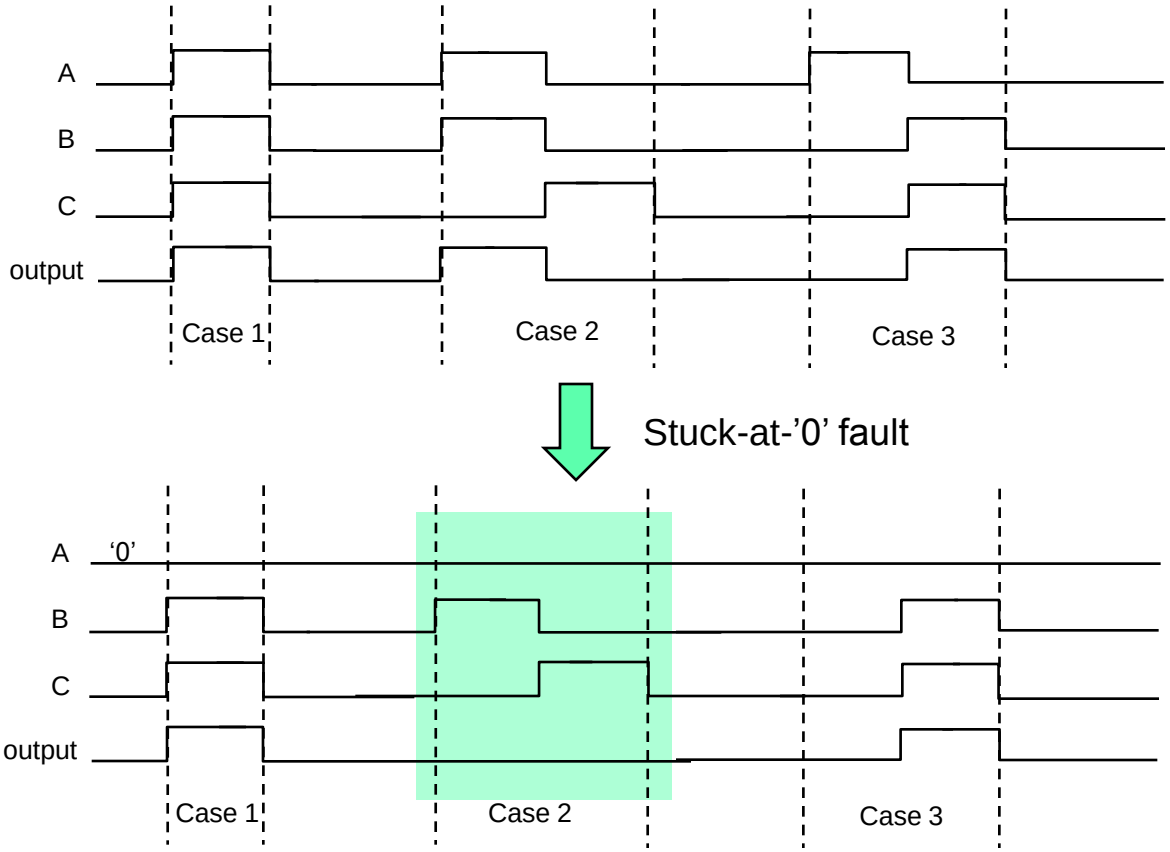
d_{max}-d_{min}=400ps, i=1,

F_s=100MHz, F_r=30MHz

disagreements = 1.2×10^6/sec

Issue #3: SEUs

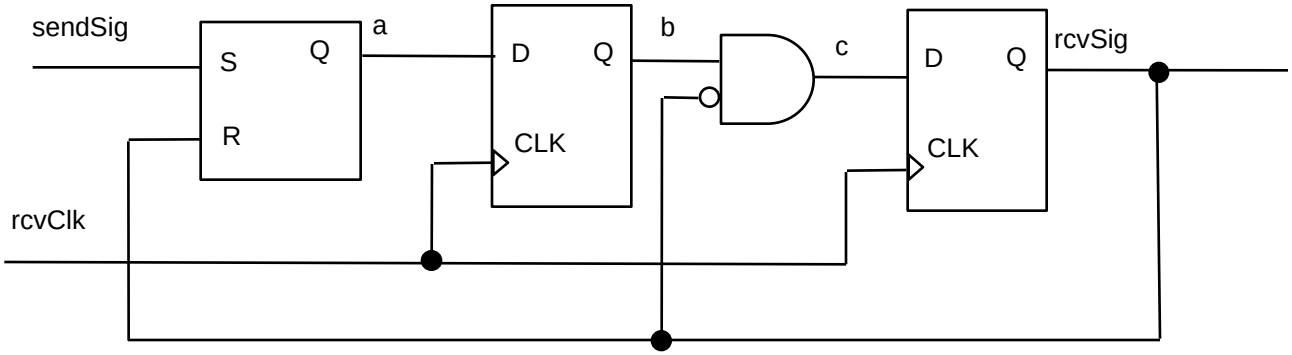
- SEUs + sampling uncertainty ⇔ TMR failure



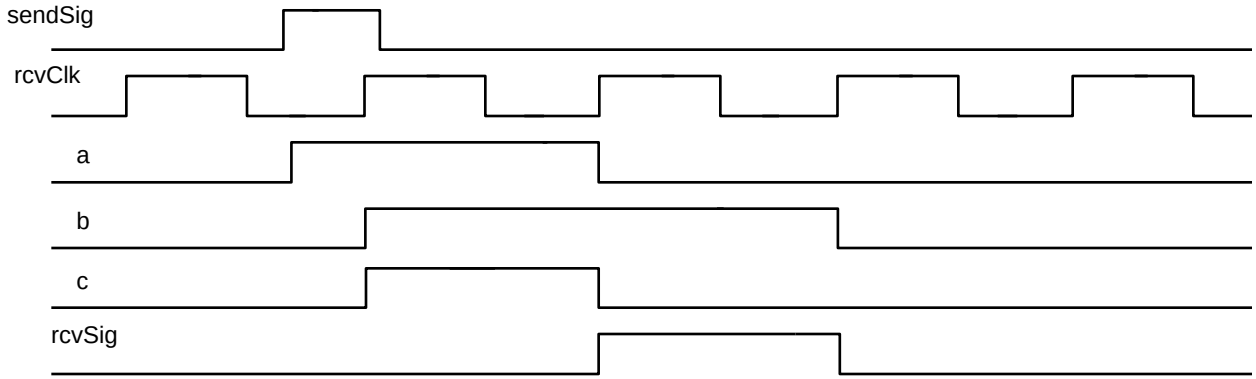
w/o SEUs

w/ SEUs

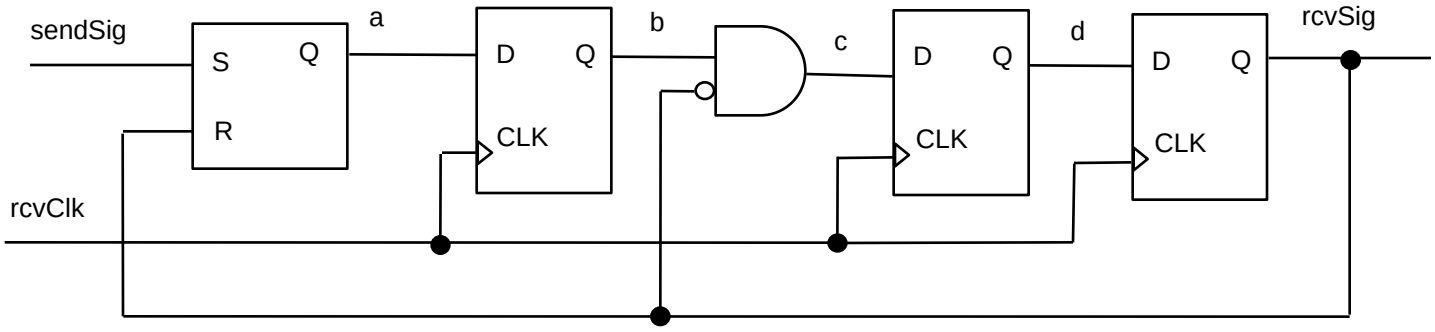
Typical Synchronizers (1/2)



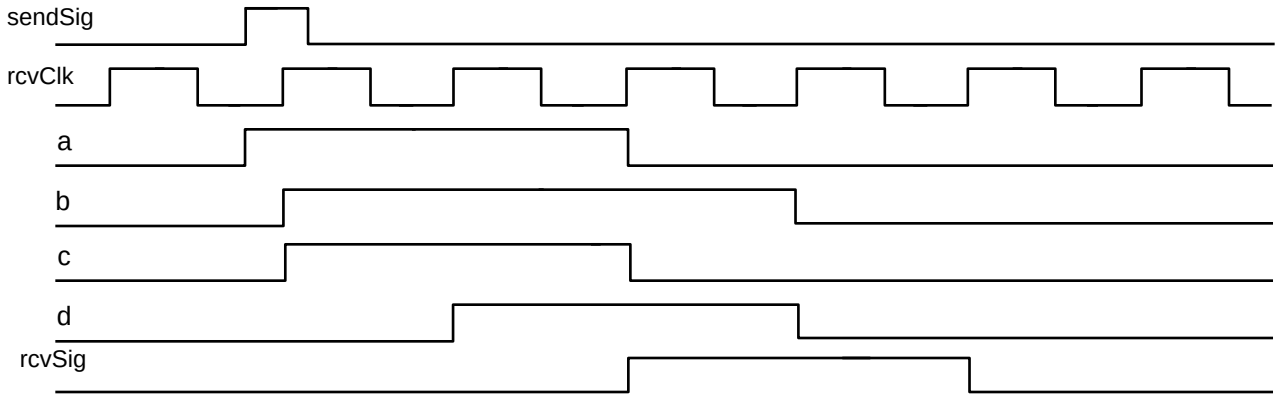
Synchronizer 1



Typical Synchronizers (2/2)



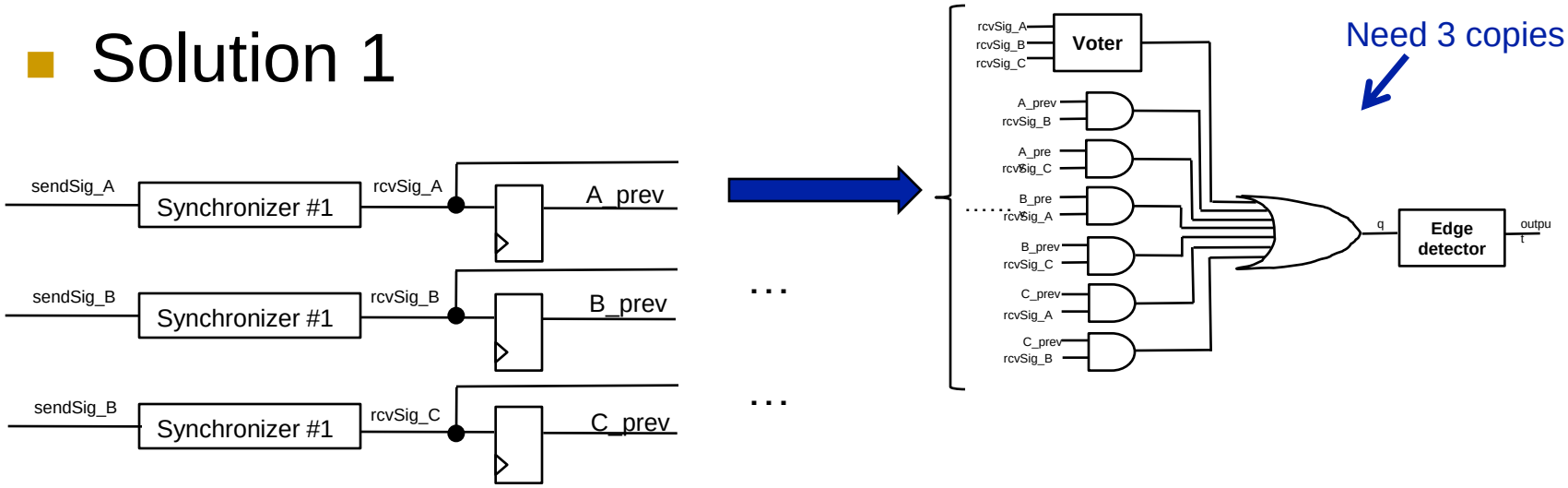
Synchronizer 2

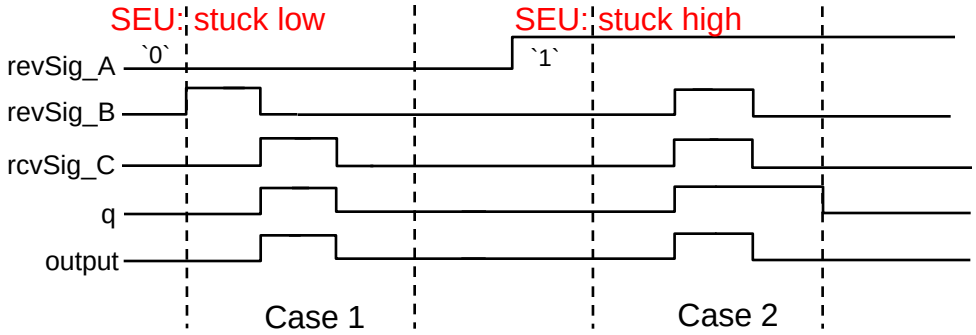


Mitigation Solutions (1/2)

This is just a 6-LUT + flip flop.

- Solution 1

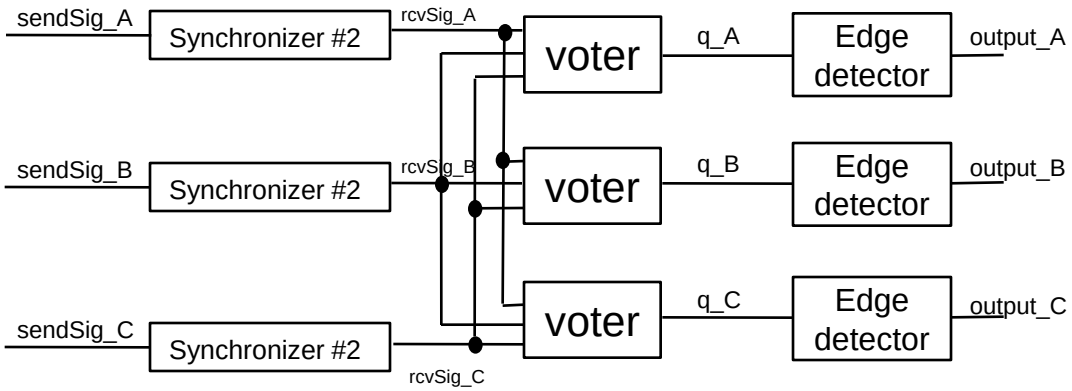


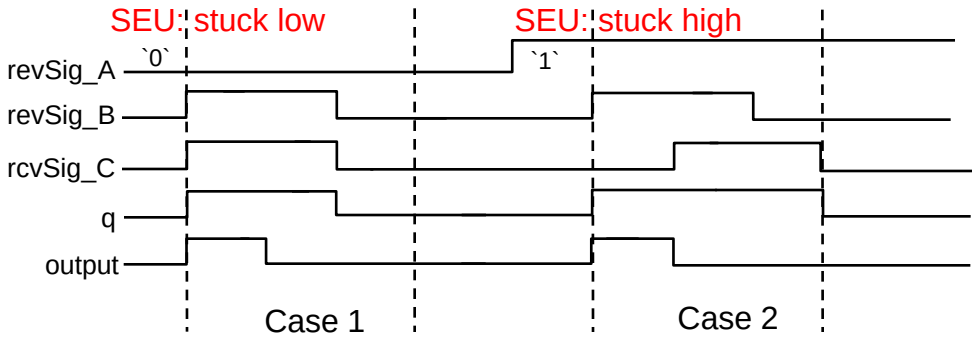


w/ SEUs

Mitigation Solutions (2/2)

- Solution 2

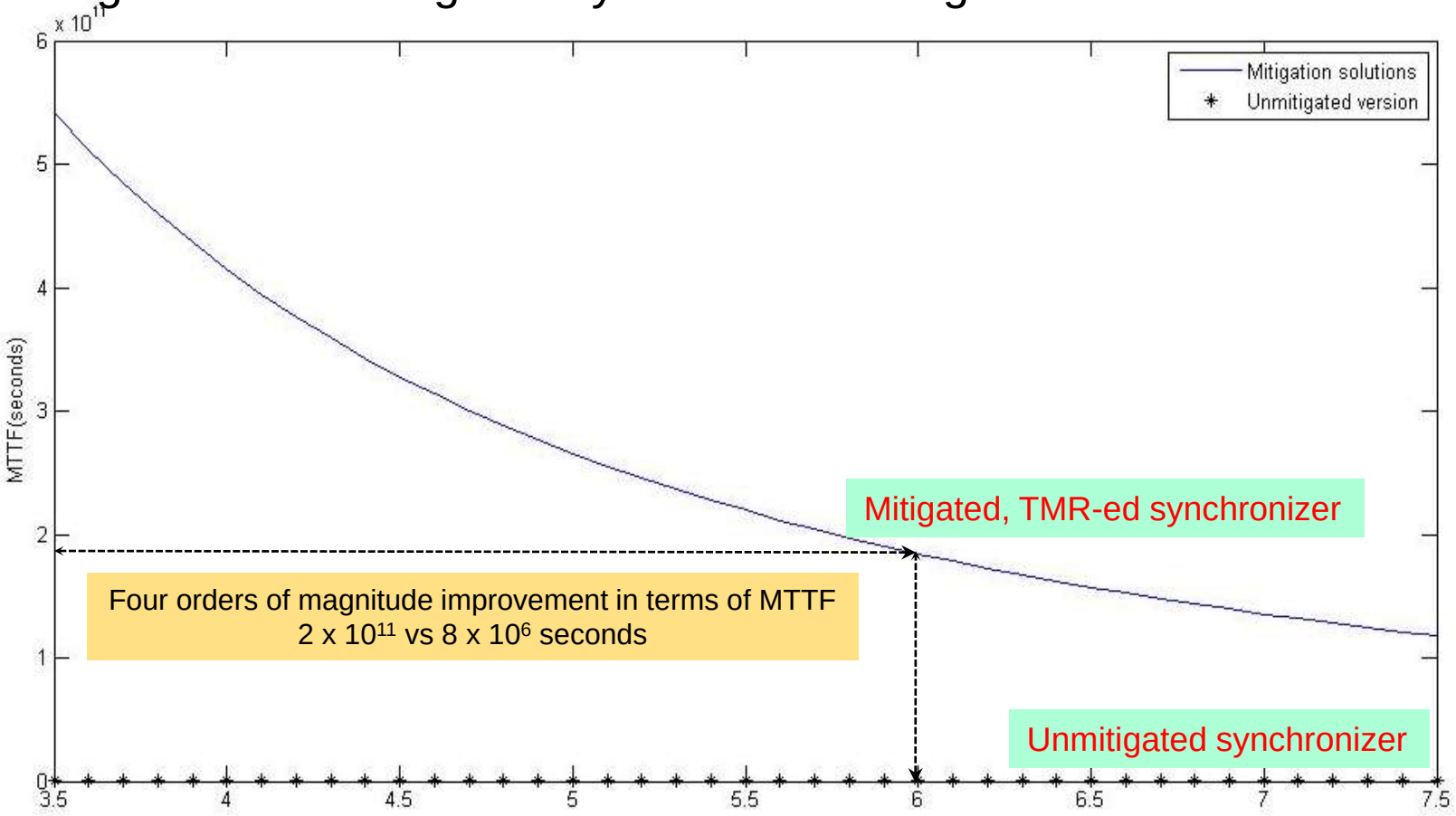




w/ SEUs

Reliability Comparison

- Mitigated vs. unmitigated synchronizer designs



X-axis: size of mitigated ÷ unmitigated

Moving Forward

- Move to more complex architectures
  - Hand-shake protocols
  - Bundled data
  - Asynchronous FIFOs
- Demonstrate reliability improvement of synchronizers using fault injection

Q&A

- Questions?