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CHREC
NSF Center for High-Performance Reconfigurable Computing

CSP Hybrid Space Computing

For STP-H5/ISEM on ISS

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Research Partners

UF (lead), NASA GSFC, BYU, NASA KSC, Honeywell, Space Micro, LM-SSC, SS&E and growing!

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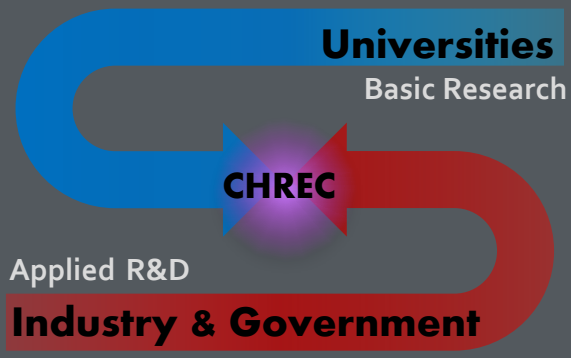
Outline

- Acknowledgements and Programs
- Brief Background of Technology and CSP
- Environmental Testing
- ISEM Configuration
- Mission Goals and Objectives
- Conclusions

CSP Acknowledgements

- CSP is a research project at CHREC
  - NSF Center for High-Performance Reconfigurable Computing (**CHREC**)
    - Founded in 2007
    - Comprises 3 university sites and **over 30 industry and government** partners
- CSP is a collaborative CHREC effort
  - Original partners:
    - University of Florida (lead), NASA Goddard, and Brigham Young University
  - Additional partners:
    - NASA Kennedy, Honeywell, Space Micro, Lockheed Martin SSC, NASA Johnson, NASA Ames, Xilinx, Space Sciences & Engineering and growing!

National Science Foundation
WHERE DISCOVERIES BEGIN



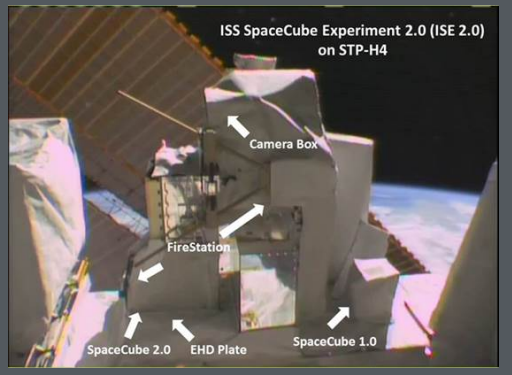
CHREC
Space Processor

See **www.chrec.org** for more info

CHREC
NSF Center for High-Performance Reconfigurable Computing

Code 587, STP-H5, ISEM

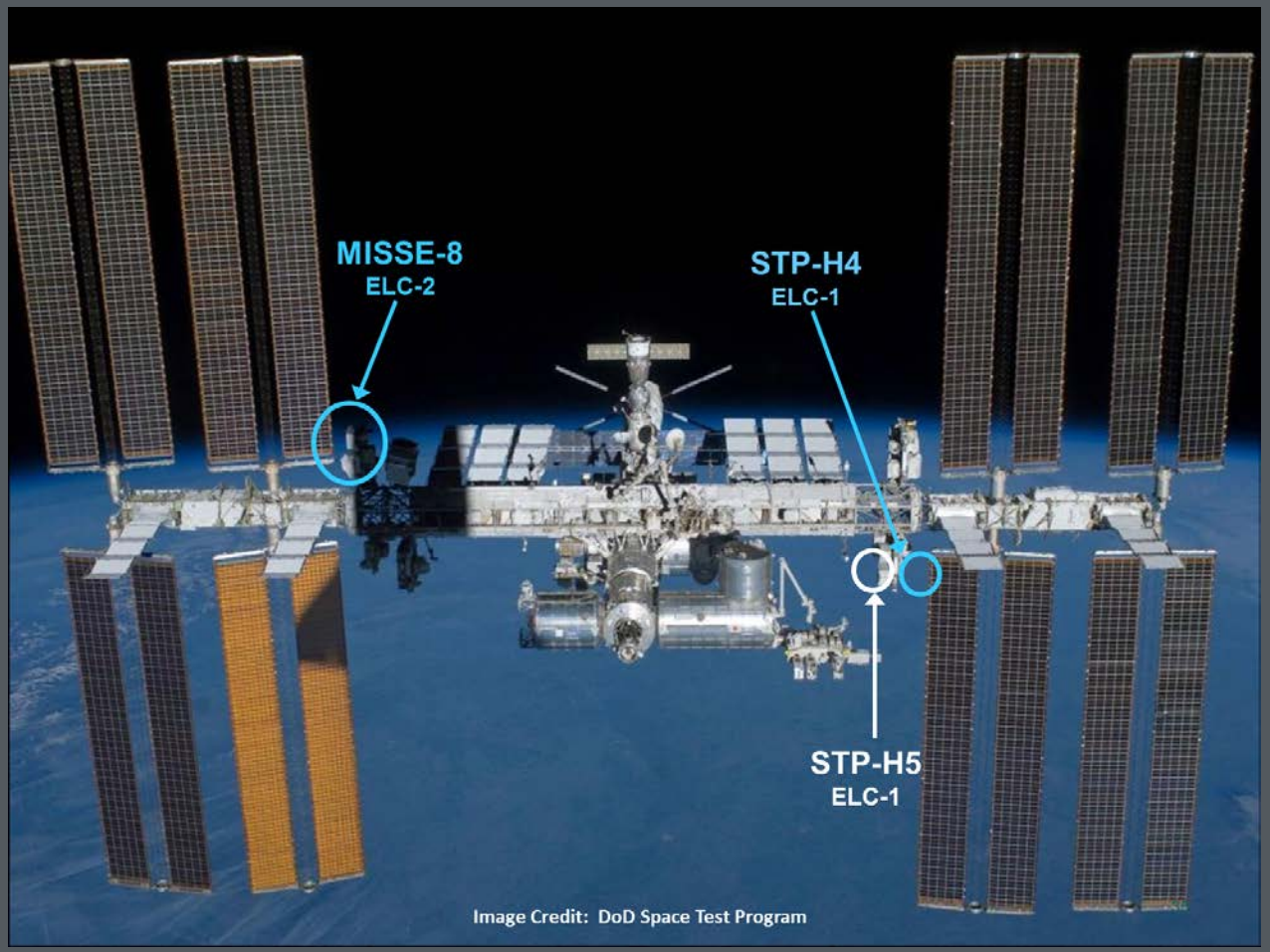
- Code 587: Science Data Processing Branch
  - Developing new technology for spacecraft architectures, mission concepts, subsystem HW
  - Provide strong science rationale for using small spacecraft platforms & constellations
  - Success with high-performance embedded computer family, **SpaceCube** (v1.0, v1.5, v2.0, and Mini)
- Space Test Program – Houston 5 (**STP-H5**)
  - Provides sole interface to NASA for all DoD payloads on International Space Station (ISS)
  - Provides timely spaceflight, payload readiness, management, and technical support for safety and integration
- ISS SpaceCube Experiment Mini (**ISEM**)
  - SpaceCube Mini is primary communication bus for some DoD payloads and CSP
  - Designed as functional equivalent of SpaceCube 2.0 in a powerful 1U package



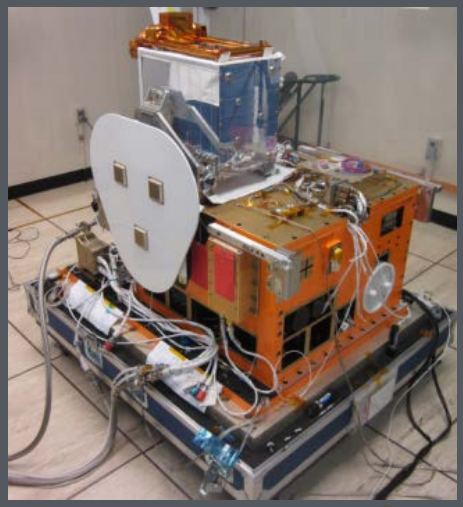
SpaceCube 1.0a

SpaceCube Mini

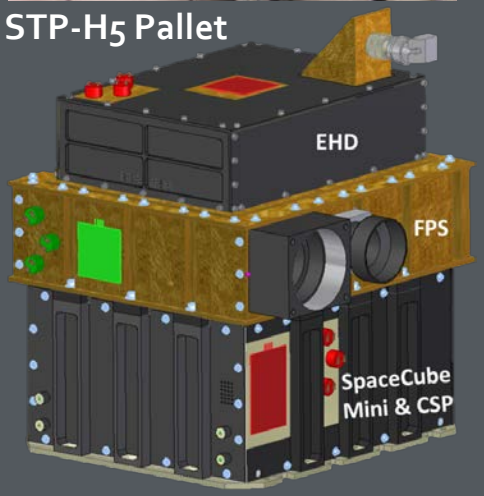
STP-H5 ISEM Diagrams



STP-H5 Location on ISS

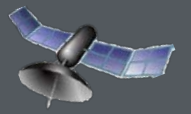


STP-H5 Pallet



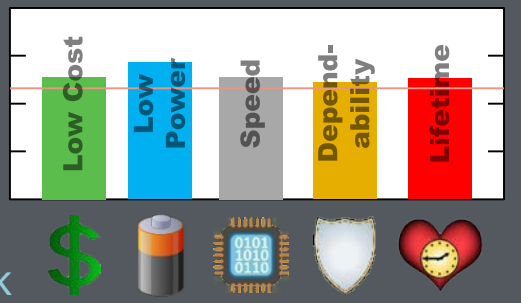
STP-H5 ISEM

Challenges and Key Terms



- Challenges
  - Escalating high-speed computing demands for both sensor-data and autonomous processing
  - Restrained by limited bandwidth

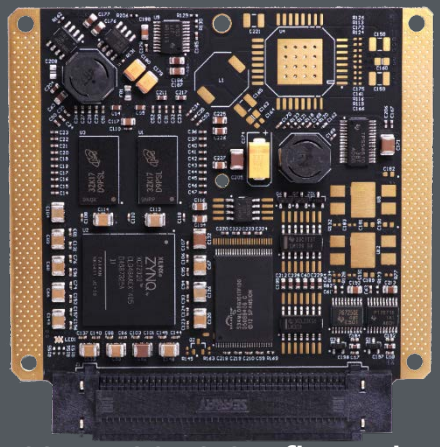
- Requirements
  - Space environments have strict requirements and restrictions
  - Performance (throughput and real-time)
  - Size, Weight, Power, Cost (**SWaP-C**)& Reliability



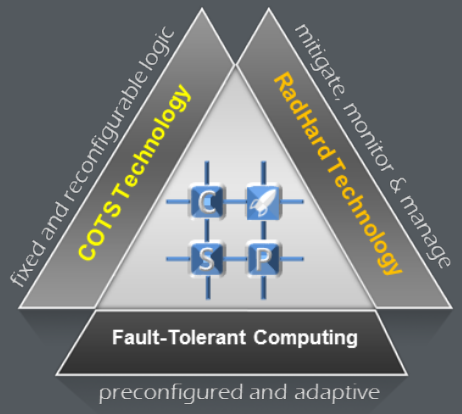
- Key Terms
  - FPGA (Field-Programmable Gate Array)
    - Large amount of logic resources and specialized cores connected with configurable routing network
    - Massive algorithm parallelism for immense speedup
  - SoC (System on a Chip)
    - Integrated circuit that combines many processing technologies into a single chip
    - Some applications are control-flow oriented and better suited for CPUs

What is CSP?

- Goal
  - Create a high-performance and reliable space-computing platform
  - Scalable and flexible to fulfill a variety of demands in mission requirements
  - Low power, high performance, and high reliability
- Concept
  - **Multifaceted** hybrid computer
    - Hybrid system (commercial + rad-hard)
    - Hybrid processor (multicore CPU + FPGA subsystem) Xilinx Zynq
  - Selective population scheme
    - **Pick-and-choose** commercial or rad-hard components
  - Flexible algorithm acceleration with hybrid architecture



CSPv1 COTS Configuration



Environmental Testing

Thermal, Vacuum, & Vibration

- ISEM required to undergo workmanship-level Random Vibration and Thermal Cycle Test
- Random Vibration Test
  - Performed to identify latent defects and manufacturing flaws in hardware
- Thermal Vacuum
  - To confirm expected performance of device in temperature ranges enveloping mission conditions
  - Two cycles in vacuum with full functional tests at each plateau

Random Vibration Test Levels	
20 Hz	@ 0.01 g^2/Hz
20 to 80 Hz	@ +3dB/oct
80 to 500 Hz	@ 0.04 g^2/Hz
500 to 2000 Hz	@ -3dB/oct
2000 Hz	@ 0.01 g^2/Hz
Overall Level	= 6.8 g_{rms}

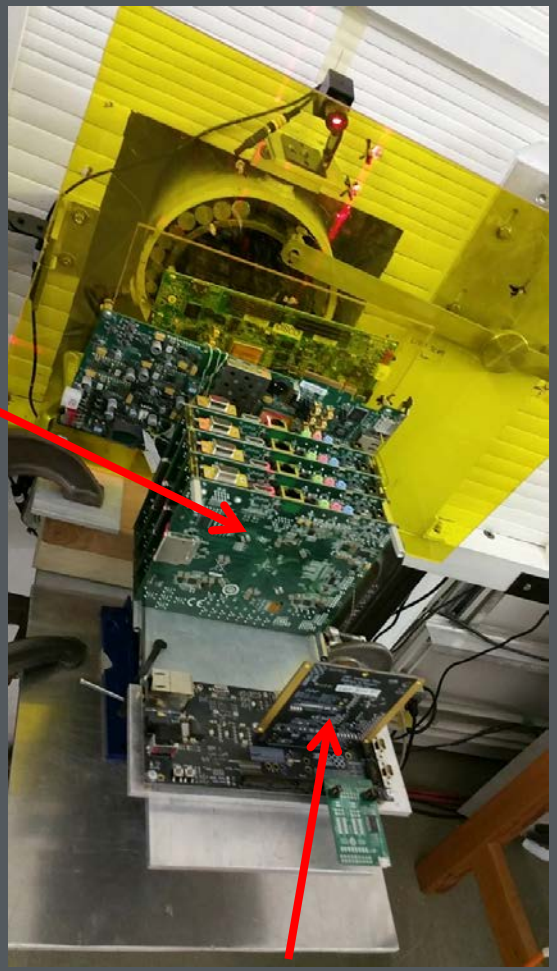
Zynq Scrubbing and Reliability

- 7 Series Scrubbing
  - FPGA configuration logic is susceptible to upsets and must be corrected continuously
  - Multiple scrubber implementations customizable to design needs
  - Bare metal and Linux applications
- Two Beam Tests Conducted
  - Los Alamos Neutron Science Center (**LANSCE**)
  - Canada's National Laboratory for particle and nuclear physics (**TRIUMF**)
- Hybrid Scrubber Verified
  - Single and multi-bit upsets observed

HYBRID SCRUBBING LOG OUTPUT:

```
Even Multi-Bit Upset, FRAD: 401B99, Global: 0
Scrubbing FRAD: 401B99...
FAULT DETECTED! FRAD: 401b99, Word: 63,
  Bit(s): 60
WORD HAD MULTIPLE BITS UPSET WITH
 2 ERRONEOUS BITS
Word: 63 | Expected: 0, Actual: 60
Scrubbing of FRAD: 401B99 Finished!
Done Scrubbing Multi..
```

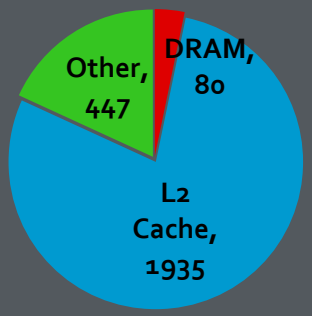
Neutron Beam Setup (TRIUMF)



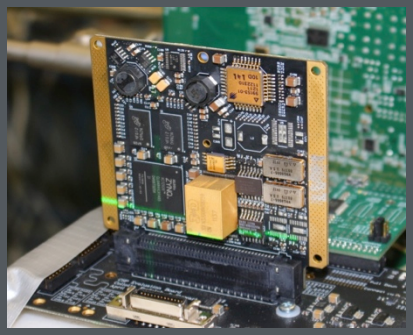
Neutron Beam Testing and Results

- Neutron CSP Results[1] (LANSCE and TRIUMF)
  - Linux readback and bare metal hybrid scrubber **verified**
  - Verified operation of rad-hard hardware watchdog
  - Most errors caused by faults in memory subsystem
- Neutron Bare Metal Zynq Test (TRIUMF)
  - Caches play a major role in system reliability
    - Difficult to measure L1 cache faults
    - "No Cache" tests had significantly lower error rate
    - Soft error rate decreased by **~160x** when disabling L2 cache

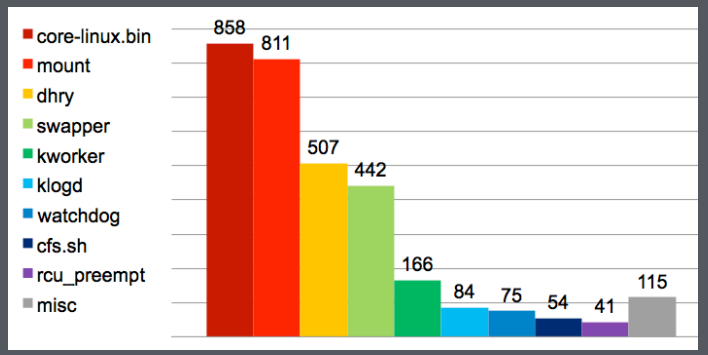
Sources of Linux Error Events (LANSCE)



Flight CSP (LANSCE) with calibration lasers



Backtrace Histogram (LANSCE) (Process/Kernel Cross section)



[1]*Neutron Radiation Test Results of the Linux Operating System Executing within the CHREC Space Processor (CSP)*, MAPLD 2015
CSP Single-Event Effect Neutron Test Results, CSP Presentation

ISEM Configuration

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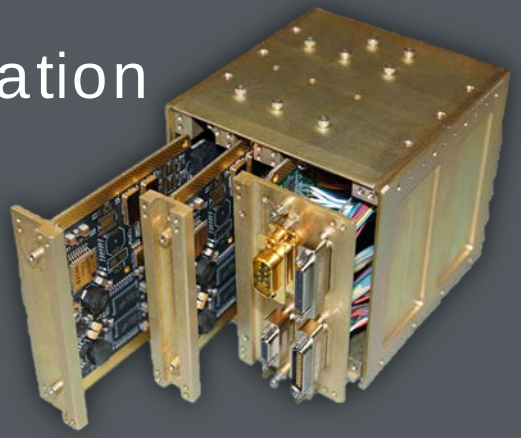
ISEM-CSP Hardware

- ISEM-CSP Flight Box Hardware Configuration
  - ISEM-CSP flight box is able to fit four boards in a 1U form-factor:
    - Two hybrid flight CSPv1 boards (CSP0, CSP1)
    - One power/interface board
    - One custom backplane interconnect board
- Connections
  - Two CSPv1 boards have a master-slave configuration
    - CSP0 receives ground commands and forwards requests to CSP1 as necessary
  - All ingoing and outgoing communication is through power/interface board
  - Backplane is central interconnect interface connecting all boards together
    - CSP0 and CSP1 are interconnected by two SpaceWire and UART interfaces

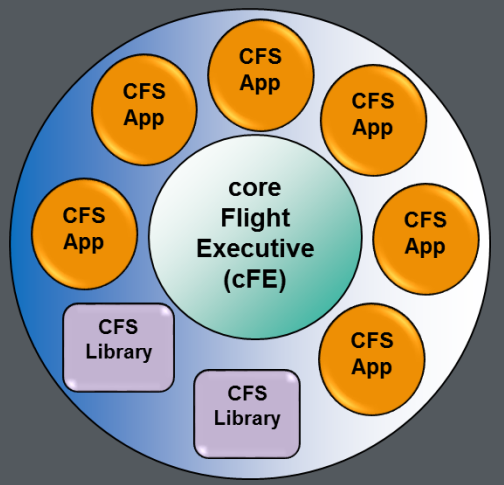


ISEM-CSP Flight Box

ISEM-CSP Testbed Setup

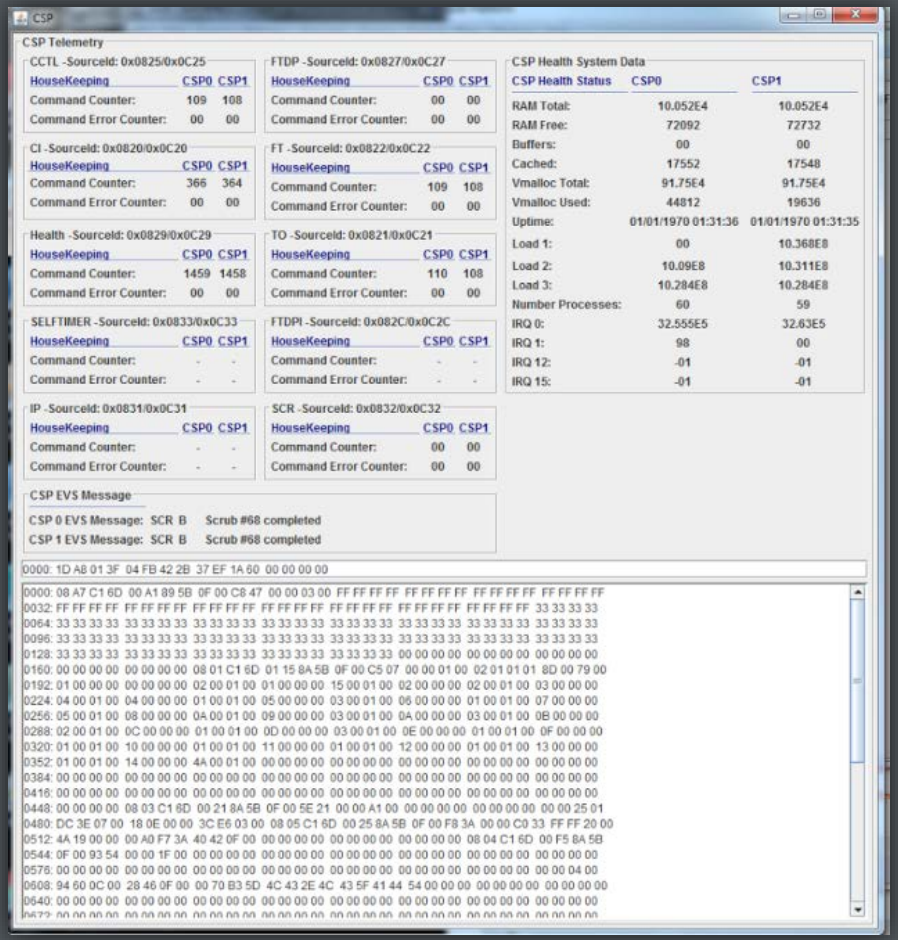
ISEM-CSP Software

- Wumbo Linux
  - Lightweight and customizable Linux distribution based initially on Arch Linux
- Core Flight Executive & Core Flight System (**cFE/CFS**)
  - NASA Goddard's **reusable** flight software framework
    - Open-source version **available at SourceForge**
    - CFS is several supporting applications and libraries
  - Added several apps for CSP
    - **File Transfers:** CIB file uploads, HRT streaming downloads, & inter-CSP transfers
    - **Image Processing:** Thumbnailing, JPEG2000 compression, & Image classification
    - **FPGA Scrubber**
- Ground Station
  - NASA Marshall's Telescience Resource Kit (**TReK**)
  - NASA Goddard's Interoperable Remote Component (**IRC**)
  - Custom Python scripts for image display

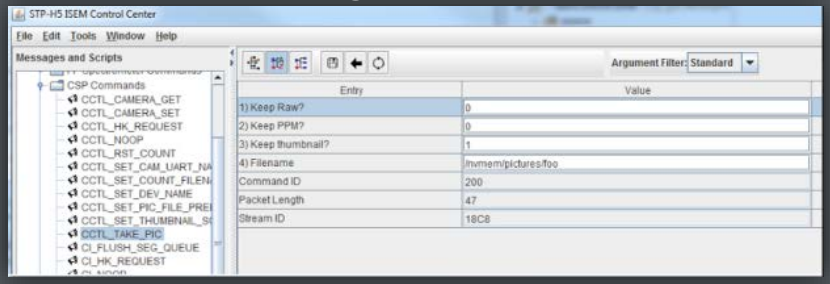


Ground Station Windows

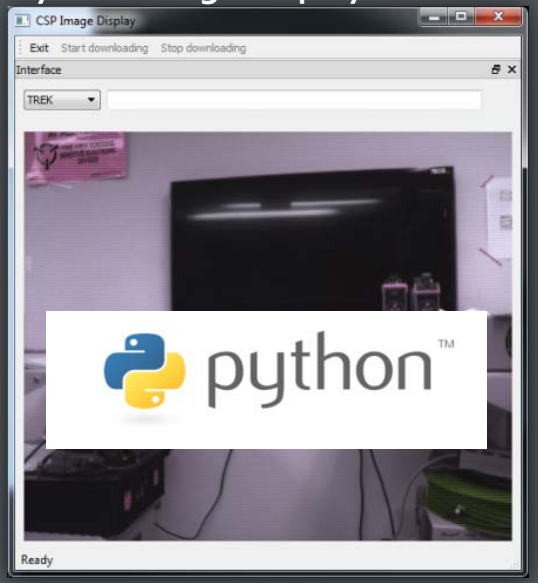
Example Health and Status Window



Example Commanding Window



Python Image Display



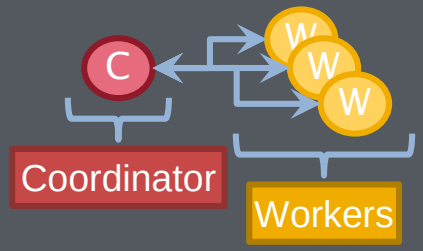
Mission Objectives

Primary Objectives

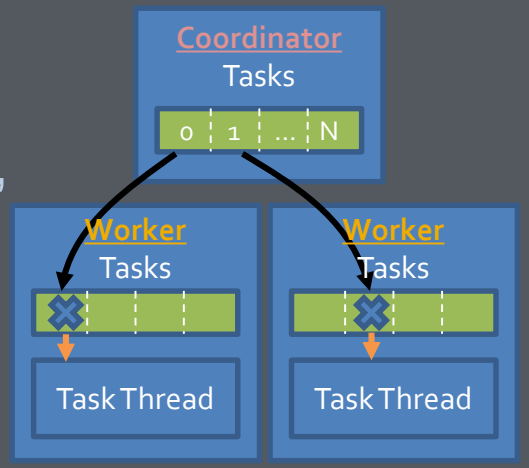
- Advance TRL of Xilinx Zynq SoC in Low Earth Orbit
  - One of many devices that are being considered for next generation of space-processing devices
- Monitor and record upset rates of both processing system (CPU) and programmable logic (FPGA) of Zynq
  - Focusing on performance of ARM cores, as well as, L1 and L2 caches

- Perform image-processing techniques including noise reduction and image enhancement on terrestrial-scene data products
  - Hardware acceleration in FPGA fabric compared with processing on ARM cores with NEON acceleration

Secondary Objective: Space Middleware - ADDAM

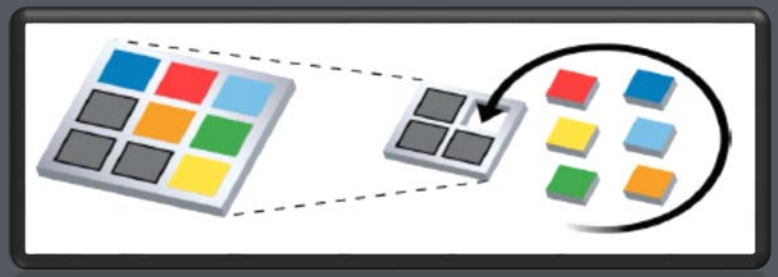


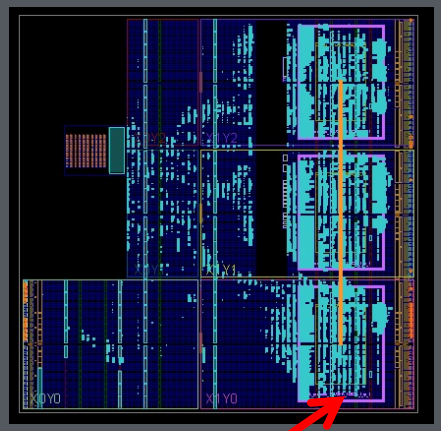
- System for dependable, distributed, and parallel computation
  - Self-recovering distributed system adopting roles of coordinator or worker as needed
  - Targeting onboard processing and task management
- Platform for building software fault-tolerance
  - Operating using task division
    - Coordinator process assigns tasks to worker process, receives results
  - Dependability through task redundancy, task reassignment for worker failure, and failover on coordinator failure
    - Supported by management threads providing fault awareness



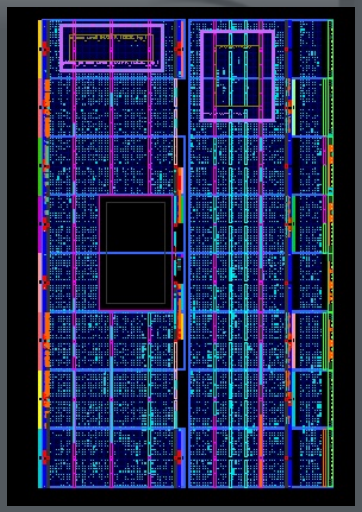
Secondary Objective: Uploads & Partial Reconfiguration

- Upload Capability
  - System software supports upload of application binaries, bitfiles, and kernel updates
  - Separate boot partition for uploading new images
- Partial Reconfiguration (PR)
  - Process of changing a specialized section of reconfigurable hardware circuitry during operational runtime
    - Mission Availability: Large suite of applications to swap in
    - Fault Tolerant Designs
    - Post-mission extendible operation with quick and seamless post-launch functional updates





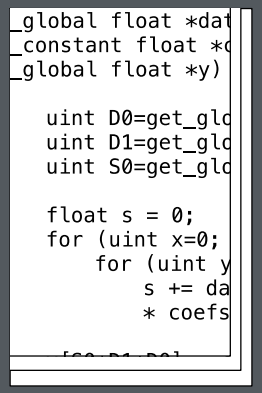
Purple Boxes Denote PR Regions

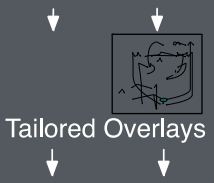


Example Designs with PR Regions

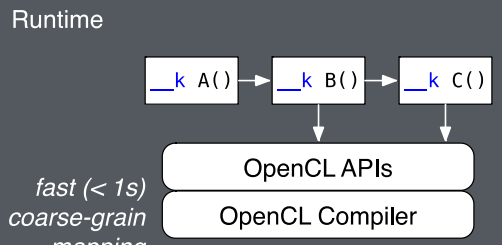
Secondary Objective: Device Virtualization

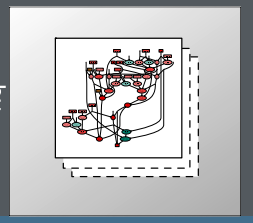
- CSP hosts new OpenCL stack using flexible accelerator *contexts*
  - Automatic design of multiple configurable, high-performance accelerators from C kernels
    - **Merges individual accelerators** into multiple PR modules to **save area**, **increase flexibility**
    - Fast (< ~1s) kernel compiles by abstracting over FPGA
    - Fast switches for resident module (1ks cycles)
  - Platform layer optimized for Zynq



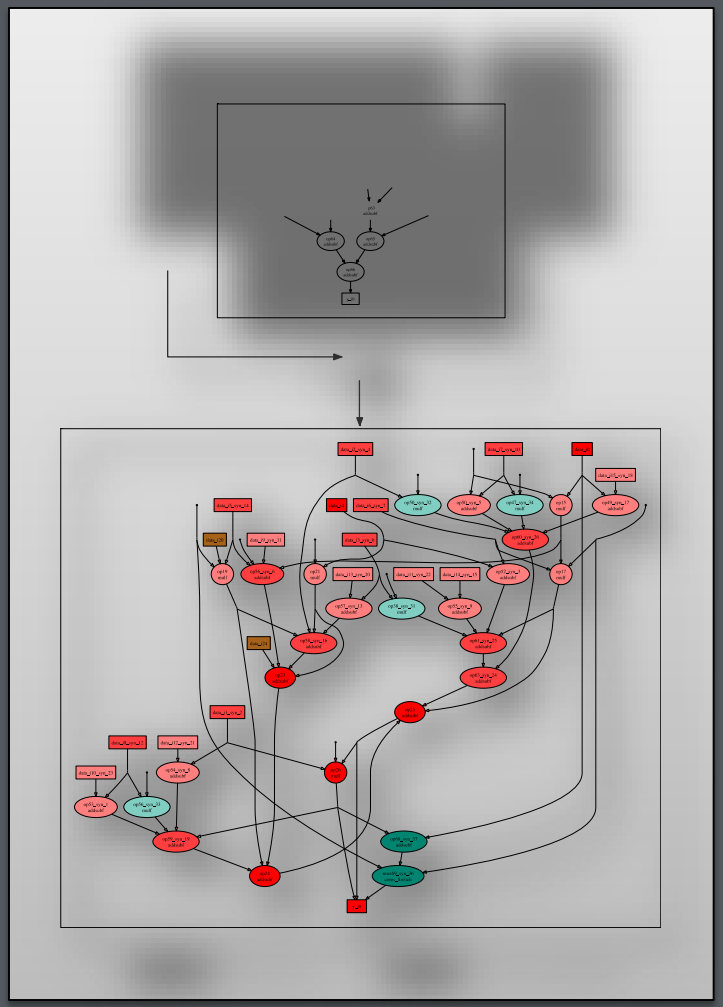


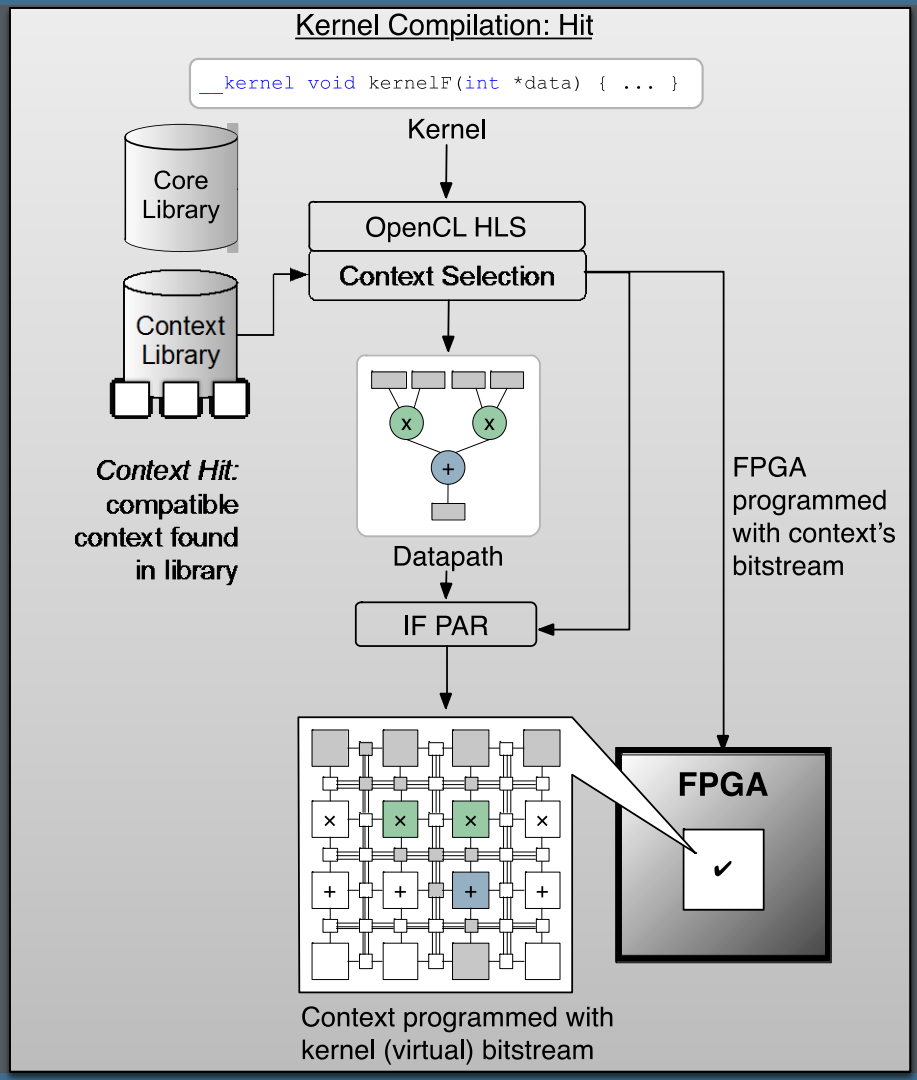
- Decouples applications/designers from details of FPGA hardware
  - Host-enforced security, energy policies (app never directly configures FPGA hardware)
  - Lifetime addition/optimization of app acceleration by uploading library patches
  - Flexibility to support dynamic optimizations





HLS with Reconfiguration Contexts and Supernets





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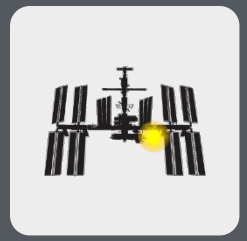
Conclusions

- **Major challenges lie ahead**
  - Escalating app demands in harsh environments
  - Tightening constraints of platform, budget, process
  - ***Necessitates adeptly doing more with less***
- **CHREC Space Processor on STP-H5**
  - Focus upon validating new CSPv1 flight design
    - Concept of multifaceted hybrid design
  - Download exciting science and technology results
    - Record vital heath & status, images, and upset rates
  - Push the bounds of possibility in space
    - Demonstrate experimental technology and methods in space with secondary objectives



More information?

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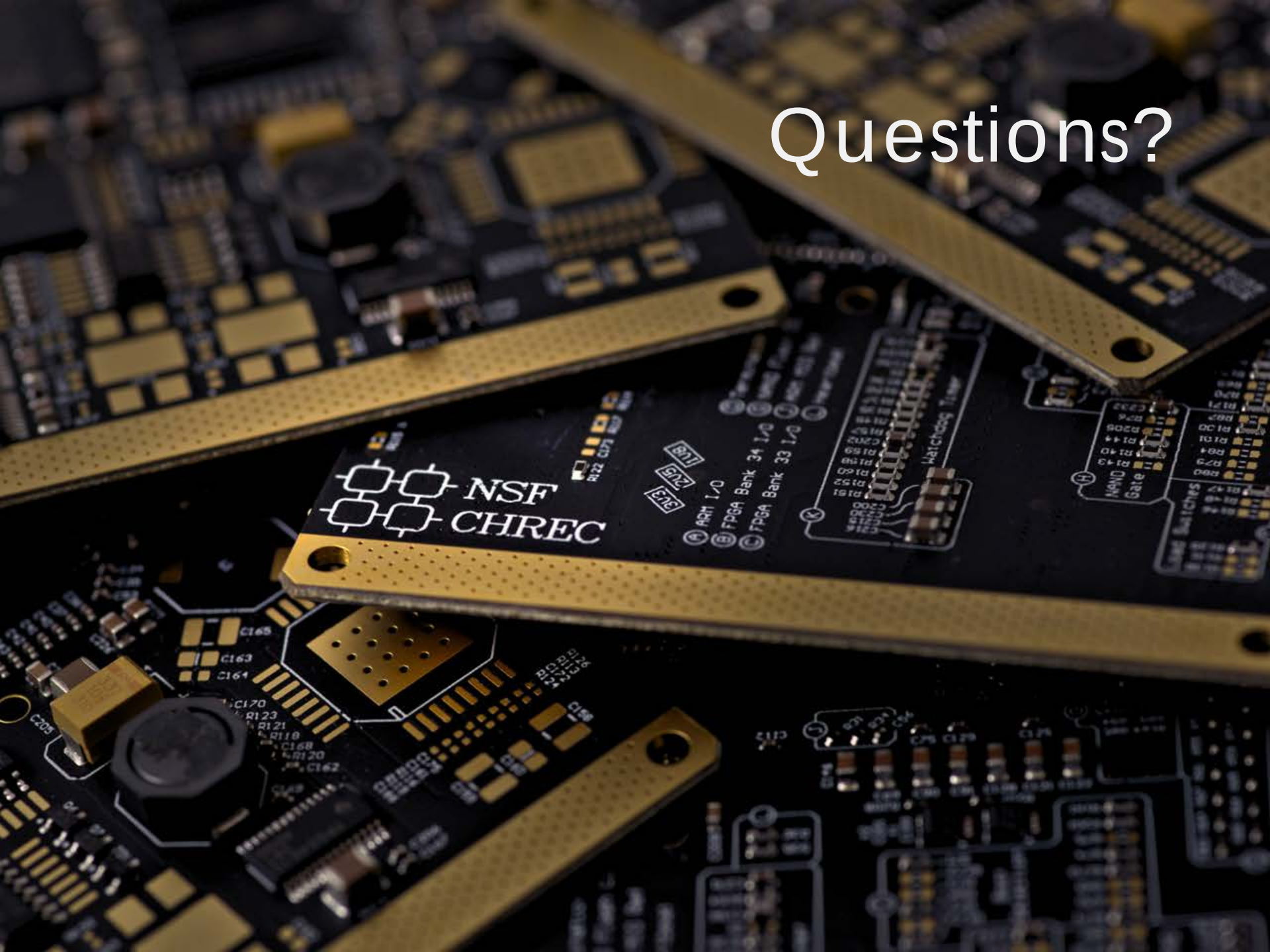
Questions?
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