Single-Event Characterization of the 28 nm Xilinx Kintex-7 Field-Programmable Gate Array under Heavy Ion Irradiation

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***Abstract*-- This study examines the single-event response of the Xilinx 28 nm Kintex-7 FPGA irradiated with heavy ions. Results for single-event effects on configuration SRAM cells, user-accessible Flip-Flop cells, and BlockRAM™ memory are provided. This study also describes an unconventional single-event latch-up signature observed during testing.**

I. Overview

THIS study examines the single-event effects susceptibility of the Xilinx Kintex-7 Field-Programmable Gate Array (FPGA). The Kintex-7 is the mid-range offering in the Xilinx 7-Series family of cutting edge FPGAs built on TSMC's 28 nm, high-κ metal gate process technology [1]. The purpose of this work is to determine the flight-worthiness and feasibility of utilizing these parts in space environments.

The part was irradiated with heavy ions at effective LETs from 1.5 to 126.1 MeV-cm^2/mg in September 2013, March 2014, and June 2014. This paper presents both single-event upsets (SEU) and single-event latch-up (SEL) results. Measured SEU results for the FPGA configuration memory, the user-accessible block random-access memory (BlockRAM™), and the user-accessible flip-flops are included.

II. Test Description

A. FPGA Device Under Test

The Kintex-7 family is offered in various configurations with different numbers of logic blocks, BlockRAM, supplemental functional features (such as high-speed transceivers, digital signal processing blocks, clock management tiles, and others), speed grade, temperature grade, packaging, and I/O pin count. Kintex-7 devices operate with a nominal 1.0 V main core voltage, an auxiliary voltage of 1.8 V, and programmable I/O pins at voltages from 1.2 V up to 3.3 V. The configuration memory in these parts is comprised of static random-access memory (SRAM) cells that control the behavior of the various internal components and the programmable interconnect [1].

The specific part tested was the XC7K325T-1FBG900C, which is a mid-range, commercial temperature-grade Kintex-7 featuring a flip-chip lidless package.

The Kintex-7 FPGA devices-under-test (DUTs) were thinned to approximately 75 μm and soldered to commercially available KC705 evaluation boards. Thinning the DUT's substrates allows even the heaviest beam to fully penetrate the active region of the silicon. The boards were verified against the KC705 OEM production test, which provided assurance that the thinned parts were installed and functioning properly.

B. Hardware Setup

In addition to the KC705 DUT, the full test setup included several important instruments located outside of the beam: an Agilent N6705B power analyzer, two USB interface pods, and a COTS FPGA board acting as a functional monitor.

The KC705 DUT board was powered through a single 12V input by the Agilent supply. The KC705 DUT board was equipped with Texas Instruments UCD9248 smart power controllers which communicate through one of the two USB pods [2] allowing individual control, monitoring and logging of the ten Kintex-7 power rails.

The other USB pod was a temperature monitoring circuit and was attached to the temperature diode of the Kintex-7 FPGA to monitor die temperature, particularly for latchup testing. A package mounted thermocouple was also monitored and readings correlated simultaneously with the diode temperature as a validation measure.

The functional monitor FPGA board was used to monitor and drive several key DUT FPGA control signals and status outputs and provides a controllable clock source to the DUT board. This enabled the clock to be easily removed for static SEU testing and to halt, as needed, synchronous switching activity for steadier current draw measurements.

C. Particle Beam Properties

The Kintex-7 DUTs were irradiated in air at the Texas A&M (TAMU) K500 Cyclotron, and in vacuum at the

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Lawrence Berkeley Laboratory (LBL) 88-inch Cyclotron. Utilizing both facilities, aluminum degraders when available, and DUT angle controls, a number of effective LETs ranging from 1.9 to 126.1 MeV-cm^2/mg were obtained. The beam parameters are shown in Table I.

TABLE I
BEAM PARAMETERS UTILIZED FOR SEU AND SEL TESTING

Facility	Effective LET [MeV-cm^2/mg]	Initial LET [MeV-cm^2/mg]	Angle [deg]
TAMU	1.9	1.9	0
LBL	2.19	2.19	0
LBL	3.1	2.19	45
TAMU	3.9	3.9*	0
LBL	4.38	2.19	60
TAMU	6.3	6.3	0
TAMU	6.9	6.9*	0
TAMU	7.1	7.1*	0
TAMU	8.8	8.8	0
LBL	9.7	9.7	0
LBL	13.8	9.7	45
TAMU	24.2	24.2	0
LBL	30.9	30.9	0
TAMU	32.9	32.9*	0
LBL	43.6	30.9	45
TAMU	63.5	53.9	31.8
TAMU	109.1	62.6	55
TAMU	126.1	63.1	60

*=obtained with degraders

D. SEU Test Procedure

The goal of SEU testing is to examine the static SEU response of the user flip-flops, BlockRAM, and configuration SRAM memory cells in the Kintex-7. During irradiation, the clock is stopped, which masks most dynamic effects typically caused by single event transients. The post-irradiation state of the DUT compared to the starting state to yields static upset counts. SEU testing was conducted at ambient temperature and nominal voltage biases.

In order to obtain flip-flop and BlockRAM upset rates, the FPGA design loaded into the DUT was designed with numerous flip-flop chains preloaded with an "all-0s" or "all-1s" pattern. Resets were configured to either reset or preset the flip-flop to ensure that reset transients would always flip the value of the flip-flop opposite of its initialized value. The FPGA design also included all available BlockRAMs in the DUT, half preloaded to "1" values and the other half with "0" values.

Following FPGA configuration, the clock was stopped and the part was irradiated to a specified fluence or until conditions arose that required stopping the beam, typically when SEU contention caused the die temperature to rise beyond safe thresholds or caused power consumption to increase beyond the capacity of the power supply. The goal was to count events corresponding to a total fluence of 10^7 or more for each LET in order to obtain statistical significance for SEU tests. It was often necessary to achieve the target fluence by accumulating event counts from multiple shorter runs in order to avoid conditions that required stopping the run early.

Once the beam was turned off, a "capture" command is issued to the FPGA which stores the state of all user flip-flops and BlockRAM into the configuration memory. The configuration memory is then read back and saved for processing to determine the number of upset flip-flop registers, BlockRAM bits, and the configuration memory bits.

E. SEL Test Procedure

SEL testing was at elevated temperature (above 90° C) and specification maximum voltages. Some runs performed simultaneously with SEU testing were performed at ambient temperature and nominal voltages. The part was configured, logging was started to record the current consumption of each voltage rail for the duration of the run, then the device was irradiated.

Current increases that might indicate latch-up were investigated post-beam. To ensure current increases were due to latch-up and not simply SEU-induced contention, configuration scrubbing and hardware resets (through assertion of the PROG pin) were employed after the beam was turned off, since true latch-up conditions would not be cleared by either of these methods but internal contention from upset configuration cell upsets would be. To further verify any current increases are indeed latch-up, the supply voltage would be lowered low enough to release the latch-up site without losing memory contents. By lowering the supply voltage beyond a minimum "holding voltage," a latch-up site cannot sustain itself [3], so lowering the supply voltage beyond a certain threshold would be another indicator that SEL has occurred. However, care must be taken in seeking this latch-up signature as lowering a voltage too far will activate internal brown-out circuitry on the Kintex-7. Note also that classical latch-up is normally accompanied by loss of part functionality, so any loss of function would help indicate that SEL has occurred as well.

III. RESULTS

A. Configuration Memory Cell SEU

The Weibull curve illustrating the configuration memory cell cross-section is shown in Fig. 1. These curves are generated with the SERET software tool [4], which takes the experimental data points and fits Weibull curves and generates space rate estimates using CREME96-like algorithms. When analyzing the readback files from SEU runs, comparisons are masked to only include bits pertinent to device operation and to exclude dynamic content (such as user flip-flop data).

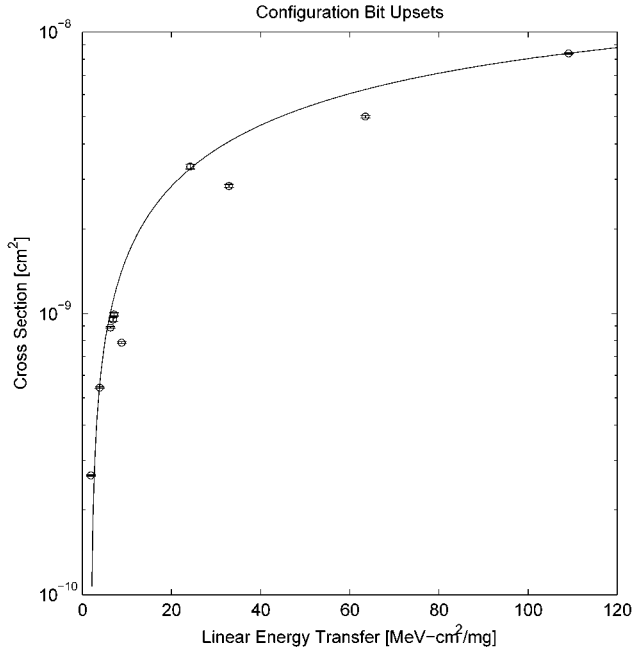

Fig. 1. Weibull curve for configuration memory cell upsets. L_{th}=1.9 [MeV-cm^2/mg], σ_{sat}=1.43e-8 [cm^2/bit], W=125.3 [MeV-cm^2/mg], S=0.78.

An investigation of upset cells revealed that memory locations loaded with 0s or 1s upset approximately equally, indicating no bias.

When investigating the location of upsets within the configuration memory space, a number of interesting multiple-bit cluster upsets (MCUs) seemed to be present. The shapes of these MCUs seemed to indicate that configuration words and adjacent logical addresses follow a physical interleaving pattern of bits between words. This interleaving is likely employed to preserve the bits used for SECDED error correction employed in the configuration words. An analysis of these multiple-bit events and their implication to inferring physical device layout is discussed in [9].

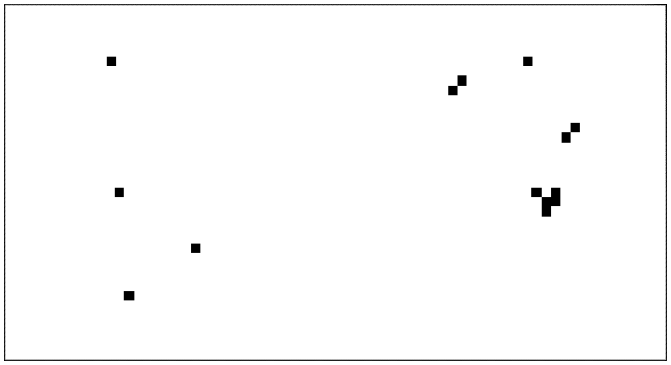

Fig. 2. Sample of MCU events mapped pictorially. Configuration words span vertical columns, and horizontally adjacent columns are logically adjacent configuration words. Some two-bit MCUs likely caused by a single strike can be observed in the upper right; note how these single-event multiple-bit events span two configuration words, likely due to physical interleaving.

B. Flip-Flop SEU

Results indicated two error signatures: (1) a flip of a single flip-flop data value due to SEU; and (2) SET-induced slice-partitioned reset.

An analysis of single-value flips from SEU (or single-cell resets) indicated no bias to flip-flops containing either 0- or 1-values. Note that because of the way the FPGA test was constructed, it is not possible to discern between a single-cell SEU causing the flip-flop value to change, or if a reset transient affecting only a single flip-flop is responsible. However, it is hypothesized that most of these single value changes are due to SEU in the memory cell and not from resets, which appear to affect larger clusters of FPGAs.

With regard to flip-flop reset transients, it appeared that resets affected flip-flops at the slice level. A number of large events were analyzed to be flip-flops that were placed within the same slice. Additionally, these events extended down and often affected other slices located in the same physical FPGA column. These reset events were observed to affect anywhere from 1 to 42 slices, but most often only 1 or 2 slices were affected. It is important to note that these observed slice reset transients are especially important for FPGA designers, as this phenomenon could be particularly defeating to design mitigation strategies (most notably TMR). Future analysis will investigate whether there is any LET dependence with respect to event size.

The Weibull curves for the flip-flop individual cell SEU and the slice reset events follow below in Fig. 3 and 4.

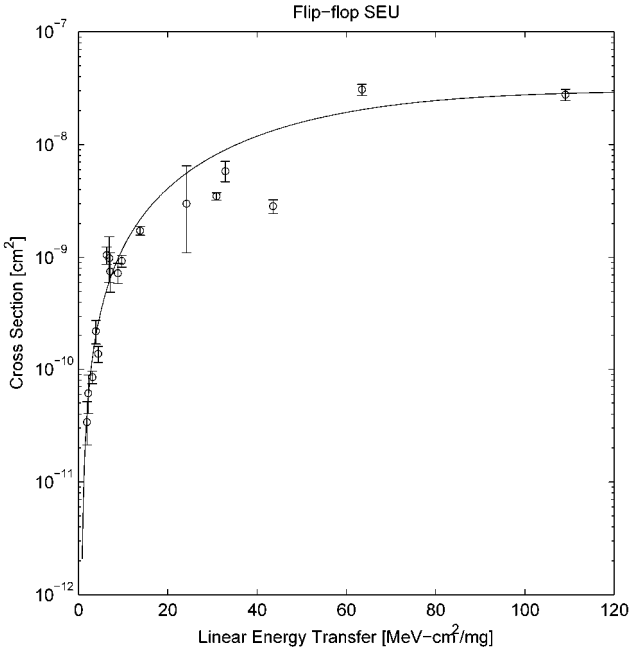

Fig. 3. Flip-flop memory cell SEU event Weibull curve. L_{th}=0.6 [MeV-cm^2/mg], σ_{sat}=3.0e-8 [cm^2/bit], W=58.4 [MeV-cm^2/mg], S=1.74.

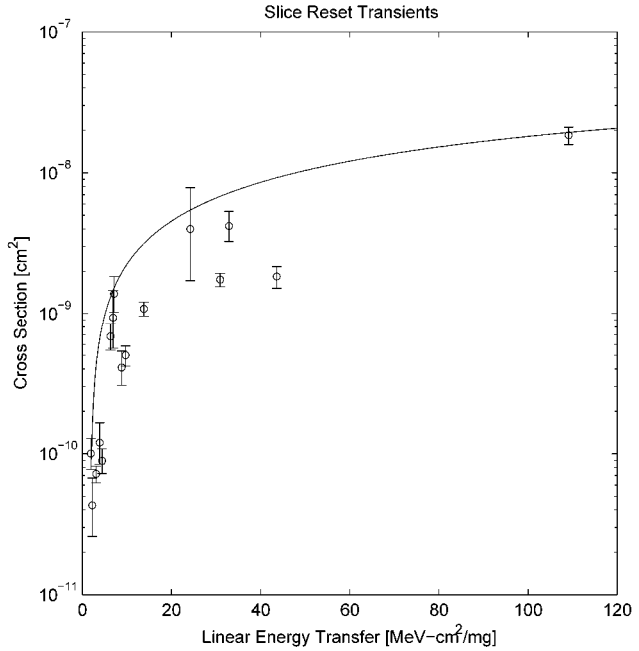

Fig. 4. Flip-flop slice reset event Weibull curve. L_{th}=1.8 [MeV-cm^2/mg], σ_{sat}=5.44e-8 [cm^2/bit], W=265 [MeV-cm^2/mg], S=0.91.

C. BlockRAM SEU

BlockRAM event analysis is ongoing, but preliminary analysis results seem to indicate that 1-values seem to upset more readily than 0-values at a ratio of approximately 5.5:1. However, more analysis and data need to be gathered before any solid assertions can be made about this imbalance. The exact cause for the bias is not known. More visibility needs to be built into the next FPGA design to allow insight into exactly how and when these BlockRAM bits are upsetting. Fig. 5 gives the Weibull curve for BlockRAM upsets.

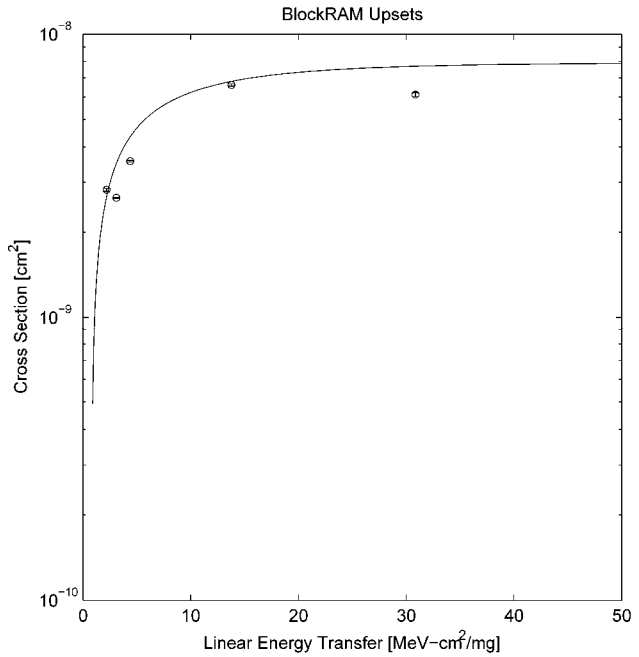

Fig. 5. BlockRAM SEU Weibull curve. L_{th}=0.8 [MeV-cm^2/mg], σ_{sat}=7.94e-9 [cm^2/bit], W=5.0 [MeV-cm^2/mg], S=0.7.

D. SEL Results

In the SEL beam runs (with high temperature and high biases), a current-step anomaly was observed on the VCCAUX supply rail at high LET. No SEL-like current signature was observed on any other rail.

The current-step anomaly resulted in multiple small current steps averaging 125 mA (σ_i = 40 mA) each. This current is quite small for classical latch-up. Additionally, no loss of part functionality was observed to accompany these single-event current steps. At low flux and high LET, the current steps are clearly discernable in captured current strip charts. One example is shown in Fig. 6, which shows 7 or 8 potential latch-up sites developing over the beam run.

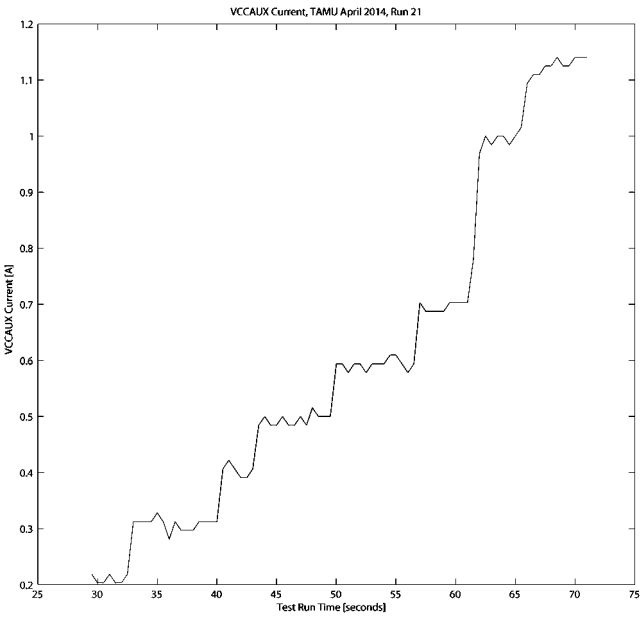

Fig. 6. Current strip chart taken during a SEL test run at TAMU, April 2014. Seven or eight SEL current-anomaly steps are clearly visible. Nominal current for this rail is 210±16 [mA].

This result necessitated careful investigation. The first mitigation steps involved configuration scrubbing, part reconfiguration, and a full reset with assertion of the hardware PROG reset pin. None of these steps resolved the additional current.

In order to verify that these current steps are indeed the result of some form of current-limited latch-up, the VCCAUX supply voltage was experimentally lowered in increments of 100 mV. Results show that dropping the voltage to 1.2 V then returning to the nominal level of 1.8 V restores the normal current state of the VCCAUX supply rail. Thus, these current steps do demonstrate the holding voltage signature of parasitic bipolar latch structures [3] and are not upset-induced internal contention or single-event functionality mode changes. What element or structure is limiting the current to such low levels is currently unknown, but under investigation.

The LET threshold of these latchup events appears to be near an effective LET of 15. Only one VCCAUX current step event is present in the data at this LET and none in any

lower LET runs. The holding voltage signature was observed for this event; nominal current was restored by lowering VCCAUX to 1.2 V then restoring it back to 1.8 V (and memory contents were retained).

The cross section for these small latch-up events is fairly small. At high LET, a device cross section of 2.9×10^{-4} cm^2 was measured. The event drops over two orders of magnitude at an effective LET of 15 MeV-cm^2/mg. The Weibull curve for this event is shown in Fig. 7.

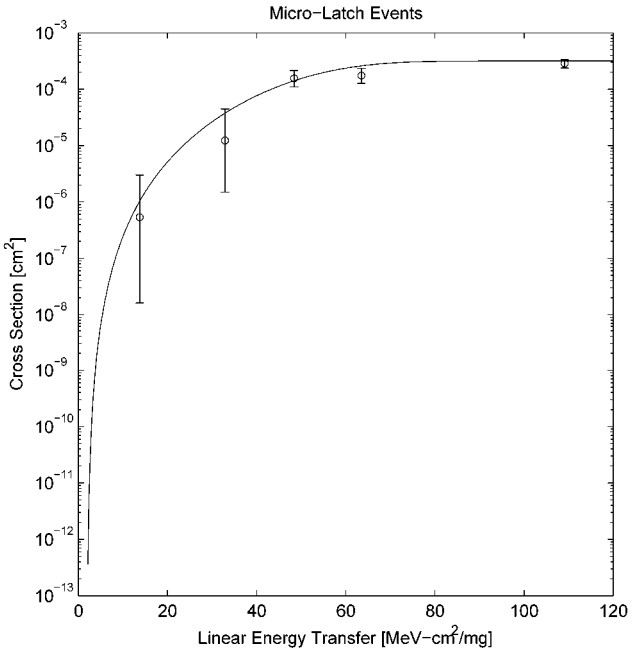

Fig. 7. Weibull curve for current-step events observed during SEL testing. L_{th}=1.9 [MeV-cm^2/mg], σ_{sat}=3.16e-4 [cm^2/bit], W=53.4 [MeV-cm^2/mg], S=3.8.

E. Event Rates

The event rates from CREME96 [8] are listed below in Table II, assuming a GEO orbit, solar minimum conditions, and 100 mils of aluminum shielding.

TABLE II
EVENT RATES FOR SEU AND SEL EVENTS

Configuration Memory	User Flip-Flops	Flip-Flop Slice Resets	BlockRAM	Current-step SEL Events
1.52E-8 /bit/day	1.33E-8 /bit/day	3.2E-8 /slice/day	2.81E-7 /bit/day	-
1.12 /device/day	5.42E-3 /device/day	1.63E-3 /device/day	4.62 /device/day	9.2E-5 /device/day

IV. CONCLUSION

The Kintex-7 FPGA parts were tested for SEU and SEL performance in heavy ions at TAMU and LBL at effective LETs from 1.9 to 126.1 MeV-cm^2/mg.

SEU cross sections are presented and performance of the part yielded reasonably good results consistent with expectations derived from combining previous Xilinx FPGA family SEU performance with transistor feature size scaling.

During SEL testing at elevated temperature and voltages, a current step phenomenon was observed at effective LETs as low as 15 MeV-cm2/mg where the auxiliary power rail showed increases of approximately 125 mA per event without any observable changes in functionality. These steps seem to be some type of low current latch-up as they demonstrate a holding voltage of about 1.2 V although no other effects were seen including any loss of function. No apparent damage was observed either. Overall, the criticality of the event seems minor, especially considering the low rate of occurrence of the event.

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